

# MS-7680 Ver: 2.0 m-ATX : 245 X 215mm

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH(H61,Co-lay H67)

## OnBoard Chipset:

HD Audio Codec:RTL887 Co-lay 892

LAN:RTL 8111E 10/100/1000 , Co-lay 8105E 10/100

SIO:FIN71869AD

Flash ROM: 32Mb SPI (PCH)

## Main Memory:

DDRIII (1066/1333MHz) \* 2 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 2

PCI Slot \* 1

## PWM:

Controller:VRD12 UP1625 3Phase

CPU+GPU: UP6282 MOSFET Driver

CPU VTT: IP6103

CPU SA : OP+MOS

DDR: UP6103

PCH: UP6103

## ACPI:

UPI

## Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX4 Front x6

USB3.0 RearX2

D-SUB/DVI/HDMI \*1

TPM Header \*1

COM Header \*1

LPT Header \*1

on BOARD BUZZER

Title Page

Cover Sheet	1
Block Diagram	2
CPU-CLK/Control/MISC/PEG	3
CPU-Memory	4
CPU-Power	5
CPU-GND	6
DDR III DIMM 1	7
DDR III DIMM 2	8
CP-PCI/E/DMI/USB/CLK	9
CP-SATA/HOST/FAN/GPIO/VGA	10
CP-SMB/LPC/AUDIO/RTC	11
CP-POWER	12
CP-GND/NVRAM	13
CP Strap	14
PCIe x16 /x1 /x1	15
PCIEx1 Slots	16
SIO-Fintek F71869AD	17
LAN - RTL8111E/8105E	18
ALC887VD_COLAY_ALC892	19
ASM1083 PCIe to PCI Bri.	20
UPD720200F1-USB3.0	21
USB3.0 Power & Connector	22
DVI transfer	23
HDMI	24
VGA	25
SATA / FAN Control	26
USB Connector	27
ACPI Controller UPI	28
DDR Power - uP6103 1-Phase	29
PCH Power - uP6103 1-Phase	30
CPU_VTT - uP6103- 1-Phase	31
CPU_SA - OP+MOS	32
VRD12 - uP1625	33
uPI6282 3-Phase CPU	34
uPI6282 1-Phase GPU	35
ATX F_Panel/EMI/TPM/LPT	36
XDP / Manual Parts	37

### 三個BOM:

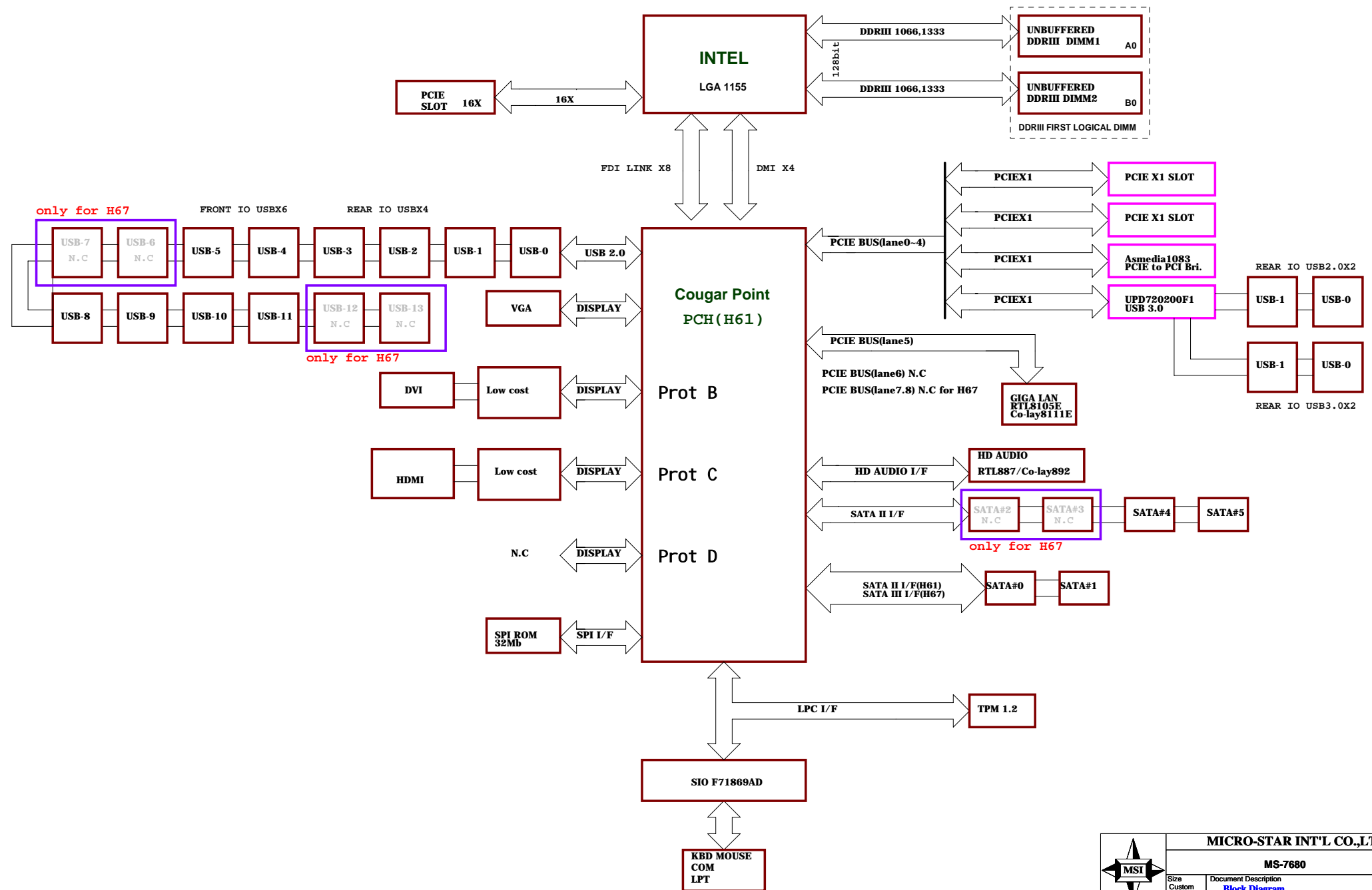
- 1.H67 Full Spec(全圖)
- 2.H61 Full Spec(全圖)
- 3.H61 common Spec(半圖)



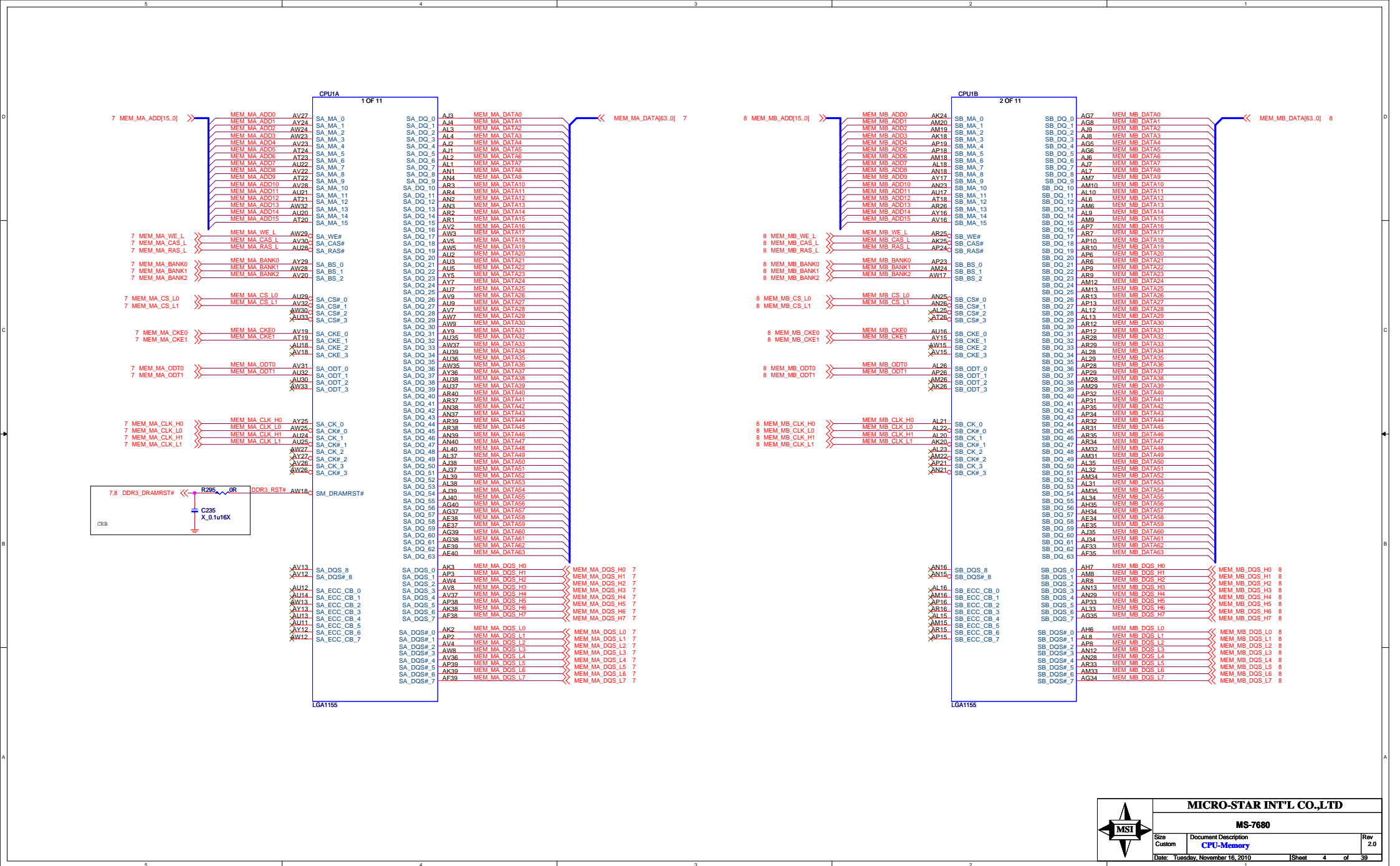
MICRO-STAR INT'L CO.,LTD

MS-7680

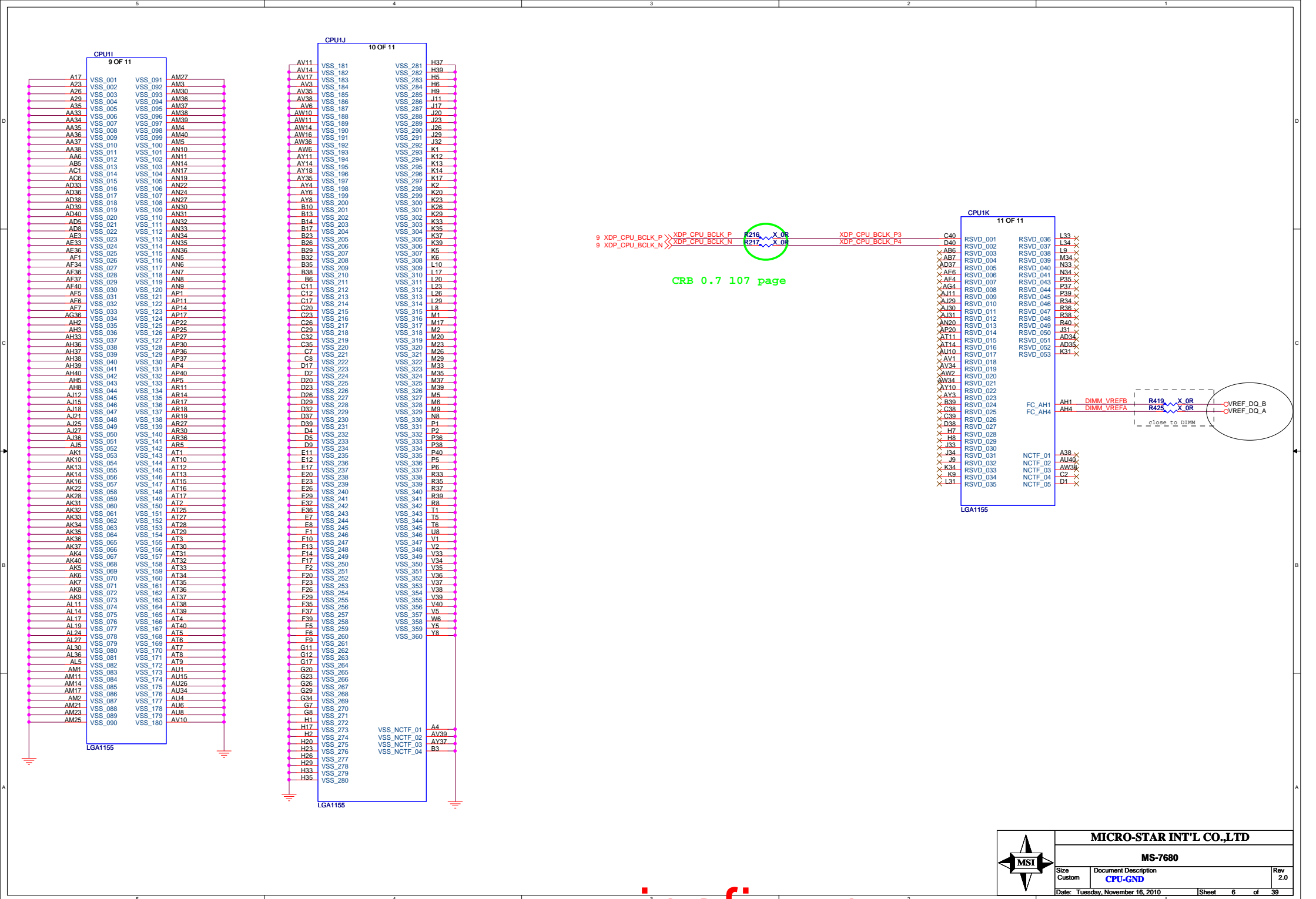
Size	Document Description	Rev
Custom	Cover Sheet	2.0
Date: Tuesday, November 16, 2010	Sheet 1 of 39	





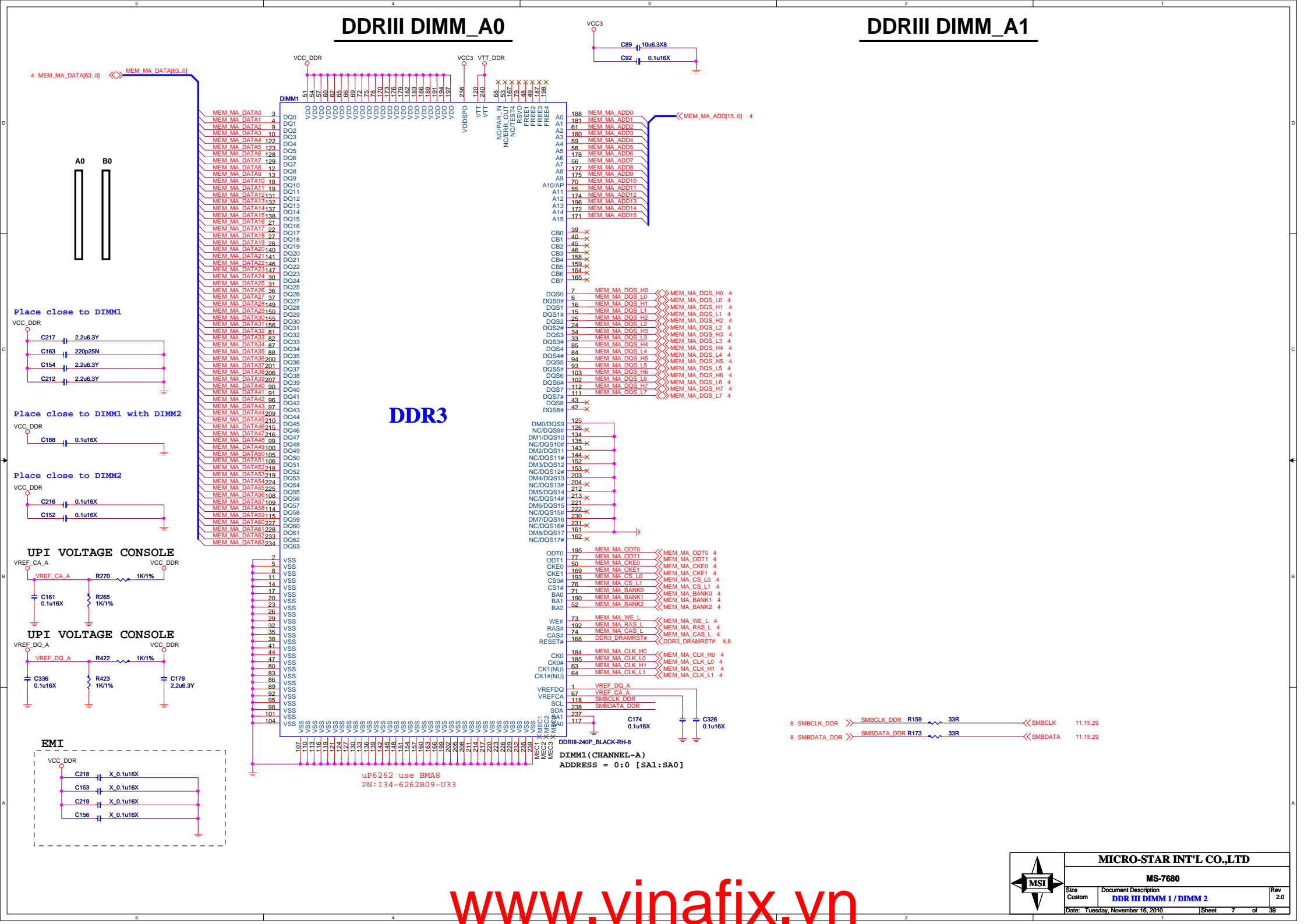




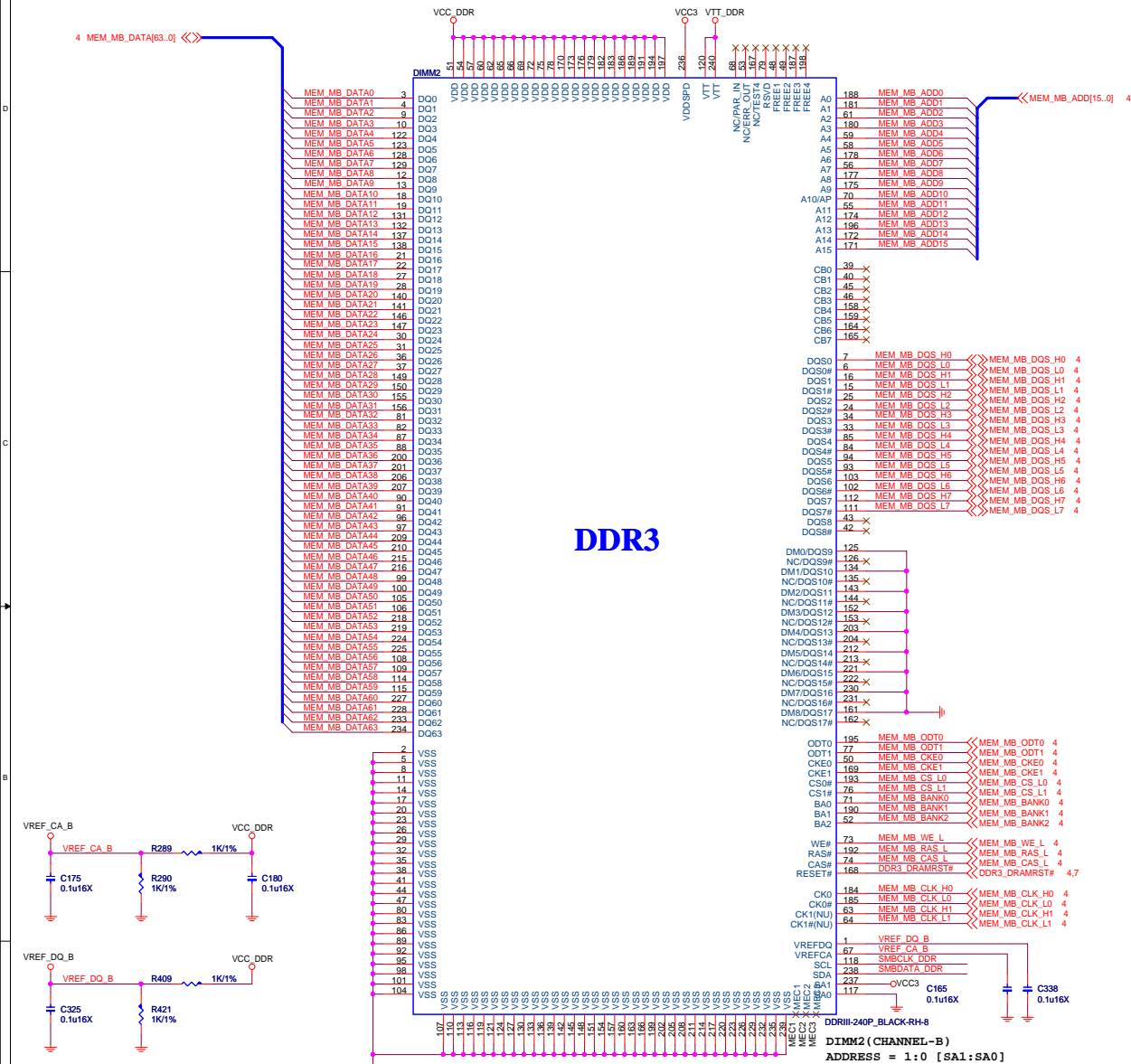


# DDRIII DIMM\_A0

# DDRIII DIMM\_A1



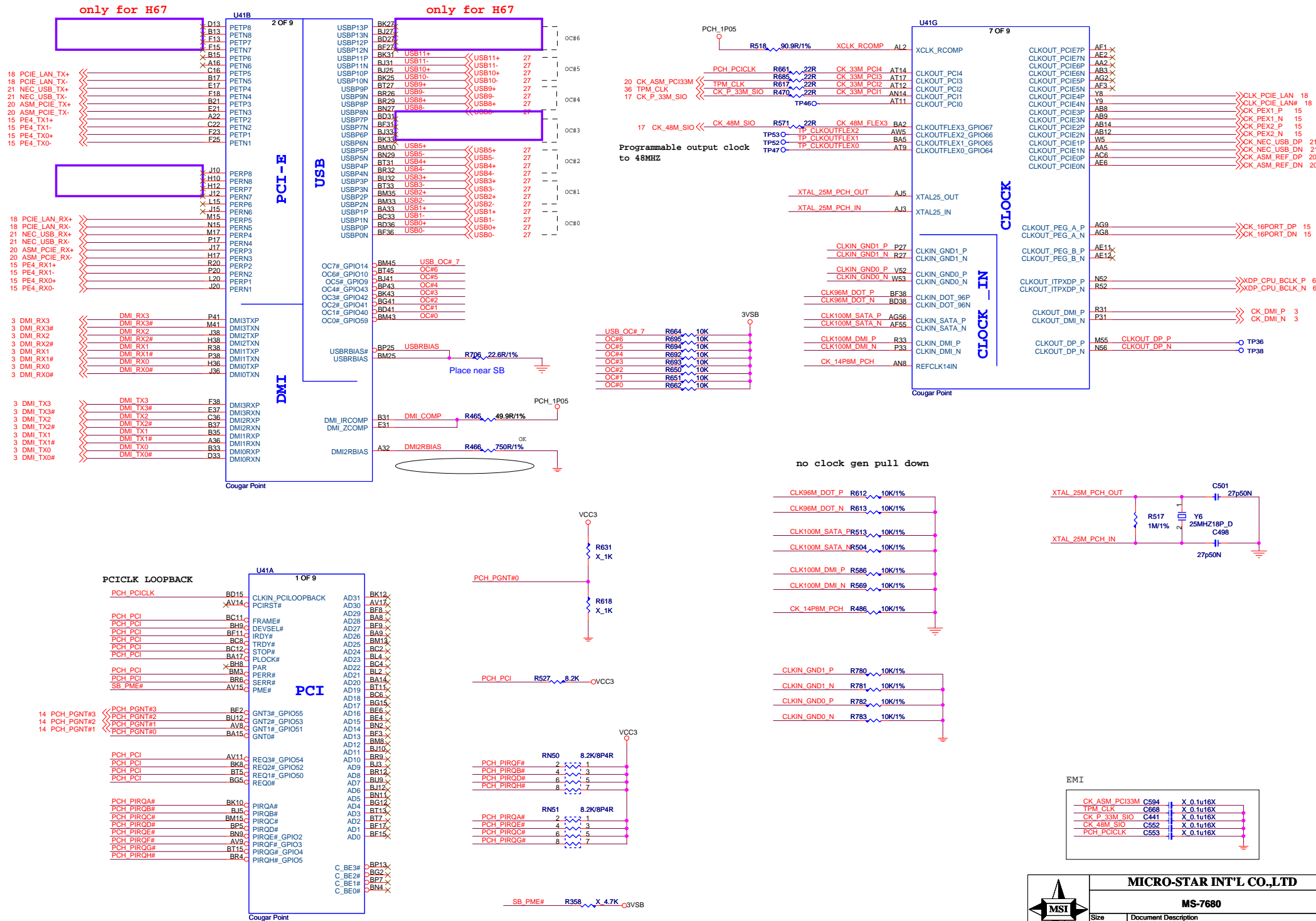
# DDRIII DIMM\_B0



DDR3

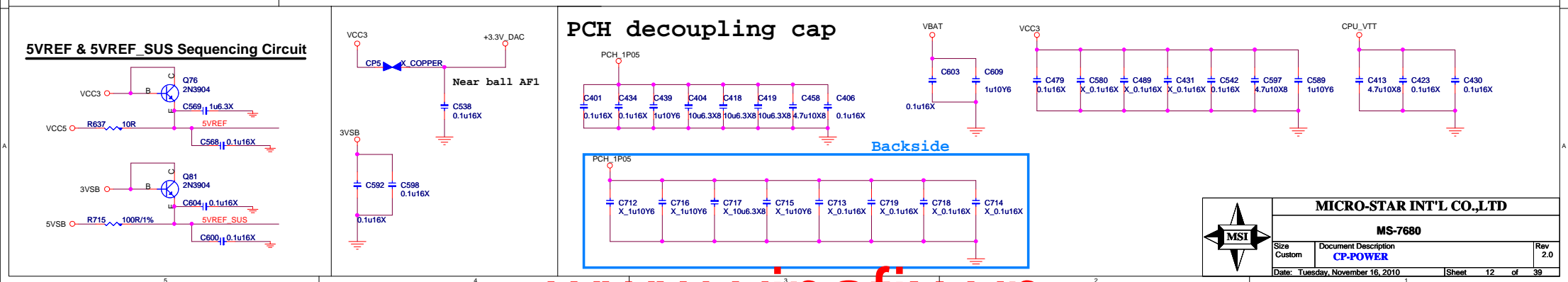
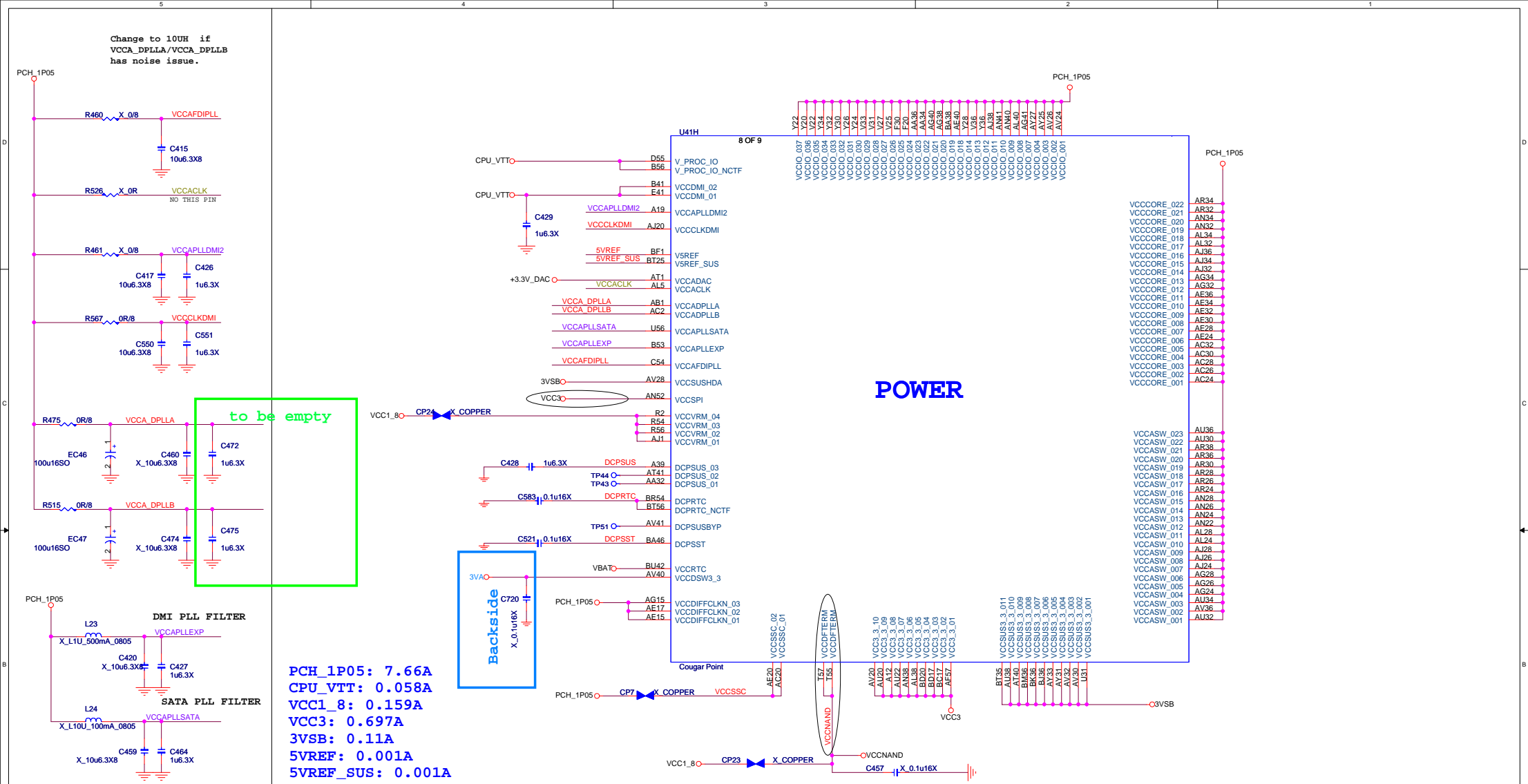
SMBCLK\_DDR << SMBCLK\_DDR 7  
SMBDATA\_DDR << SMBDATA\_DDR 7


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Size	Document Description	Rev	
Custom	DDR III DIMM 3 / DIMM 4	2.0	
Date: Tuesday, November 16, 2010		Sheet	8 of 39



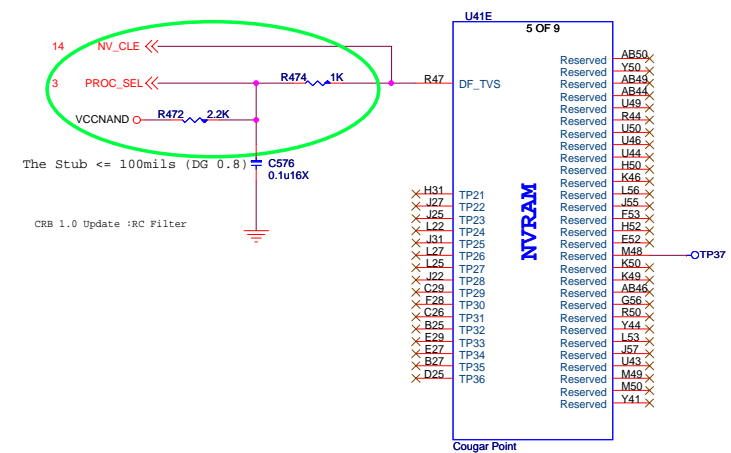
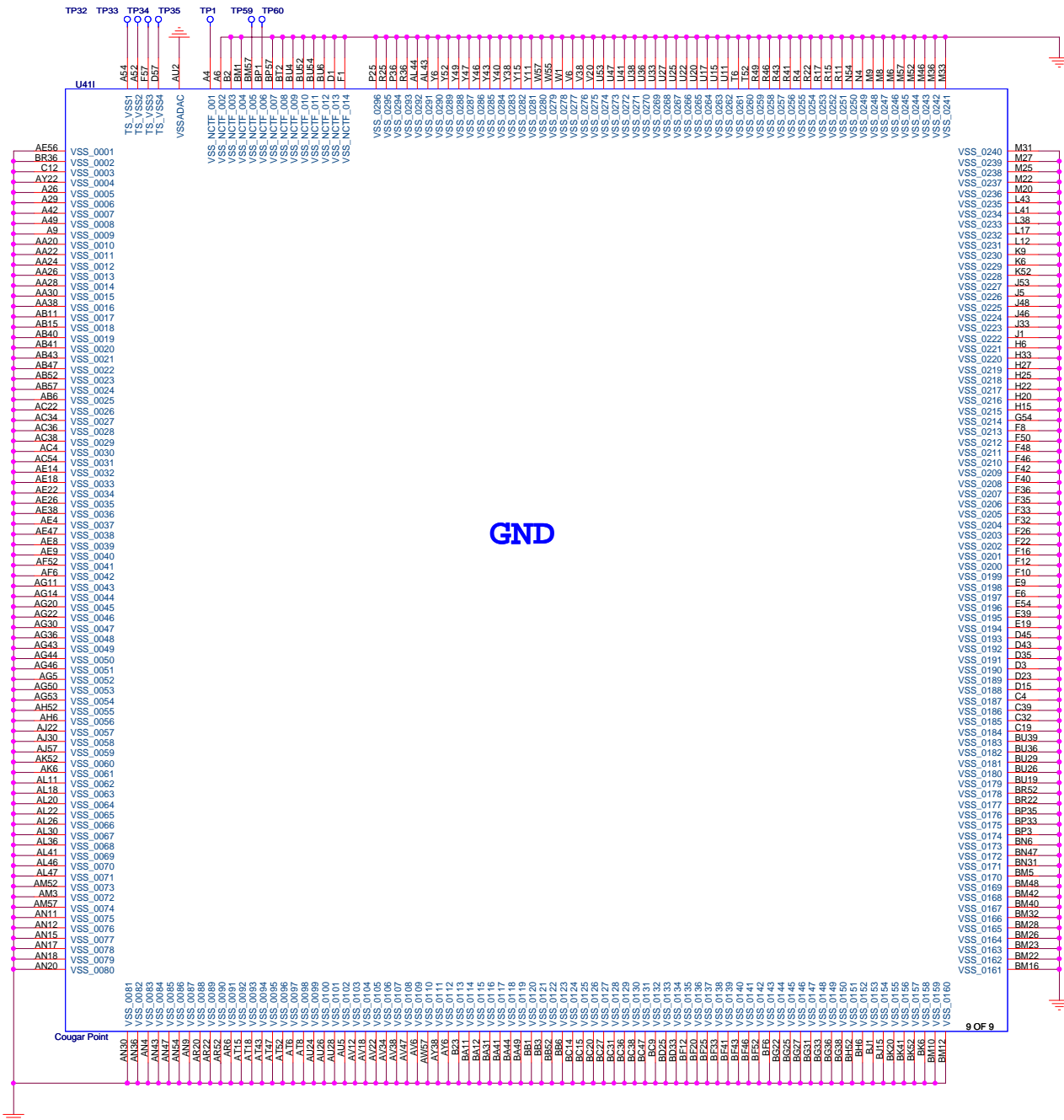






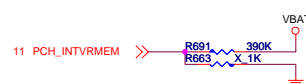
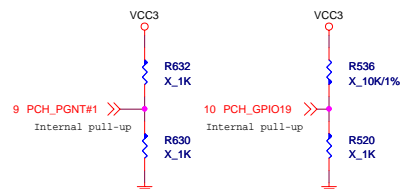


MICRO-STAR INT'L CO.,LTD			
MS-7680			
Size	Document Description	Rev	
Custom	CP-POWER	2.0	
Date: Tuesday, November 16, 2010	Sheet 12	of 39	



# PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



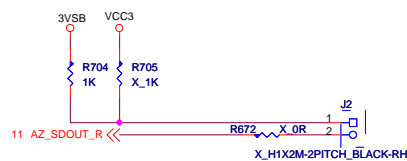
INTVRMEN  
0: DISABLE INTERNAL VRM  
1: ENABLE INTERNAL VRM \*

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.



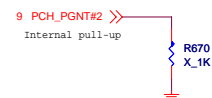
DSWVRMEN  
0 : Disable Internal Deep Sleep 1.05 V regulators.  
1 : Enable Internal Deep Sleep 1.05 V regulators.

This signal enables the internal Deep Sleep 1.05 V regulators. Must be connected even when not supporting DSW.

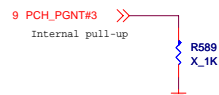


HDA\_SDO  
Disable ME in Manufacturing Mode  
when pull LOW ????

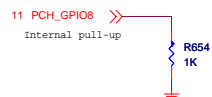
HDA\_SDO has internal pull down.  
Default should be connected to SDIN of codec, no pull up/down.  
To Disable ME need to have a jumper to pull high



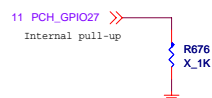
DMI AC/DC MODE  
0 : AC  
1 : DC \*



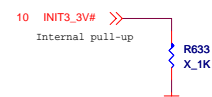
Topblock swap override when pull-low  
Signal has a weak internal pull-up



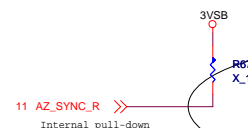
GPIO8  
0 : Integrated Clocking Enable (FCIM)\*  
1 : Buffer Through Mode Enable (BTM)



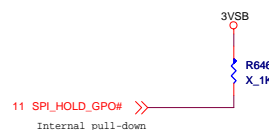
GPIO28  
0 : OD PLL VR disabled  
1 : OD PLL VR enabled \*  
Signal has a weak internal pull-up



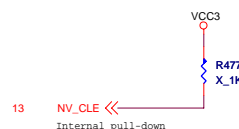
INT3\_3V#  
0 : ??????????????  
1 : ?????????????? \*



HDA\_SYNC  
OD PLL VR SUPPLY SEL  
0: 1.8V SUPPLY \*  
1: 1.5V SUPPLY



GPIO15  
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY \*  
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



DMI/FDI TERMINATION VOLTAGE  
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH  
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW \*?  
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP

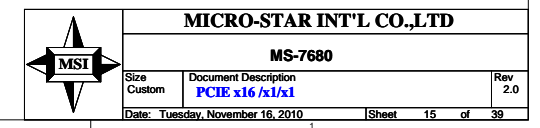
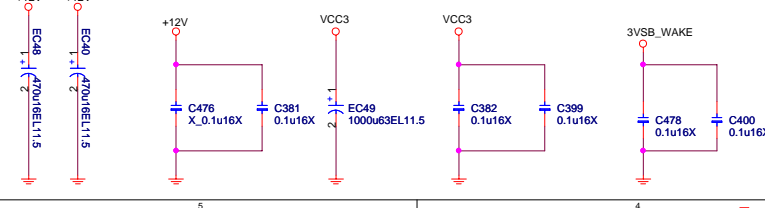
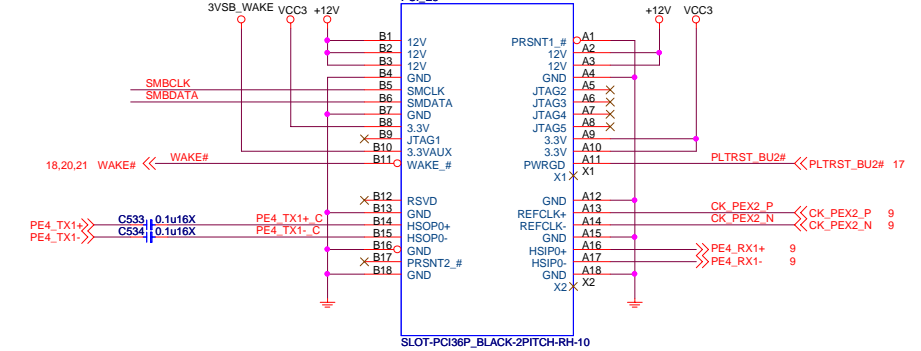
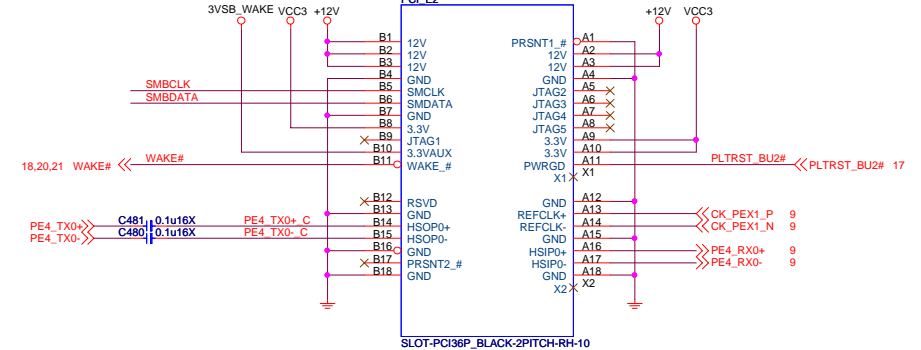
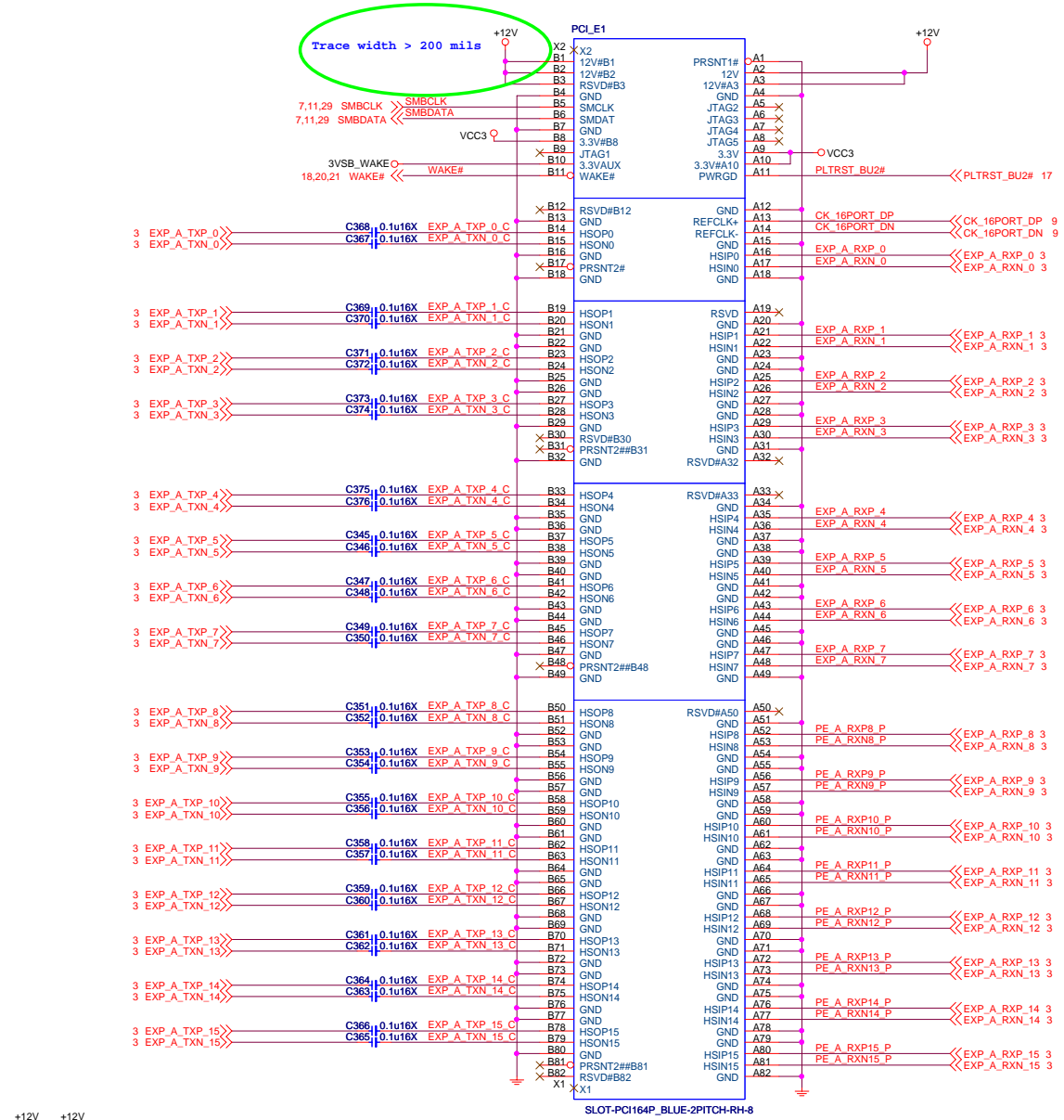


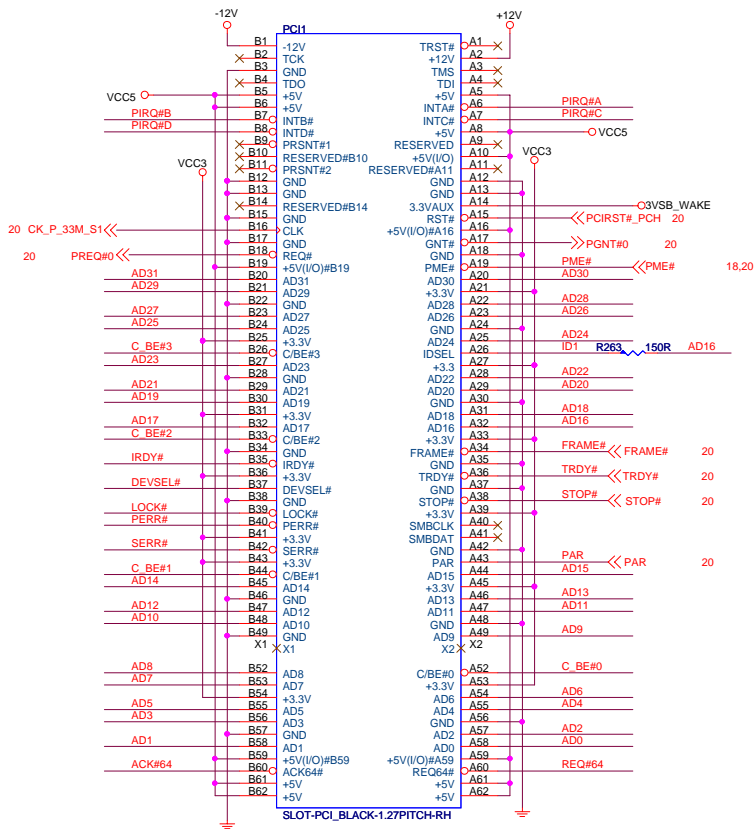
SPKR  
0 : EN TCO REBOOT \*  
1 : DIS TCO REBOOT

1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.

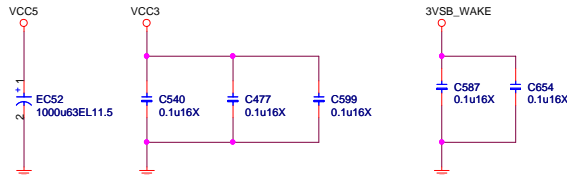
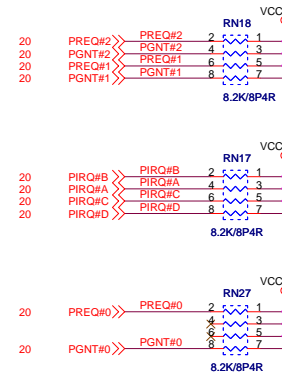
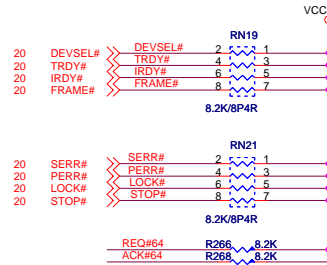
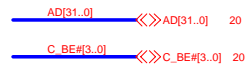
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MS-7680		
Size Custom	Document Description CP-Strap	Rev 2.0
Date: Tuesday, November 16, 2010	Sheet 14 of 39	

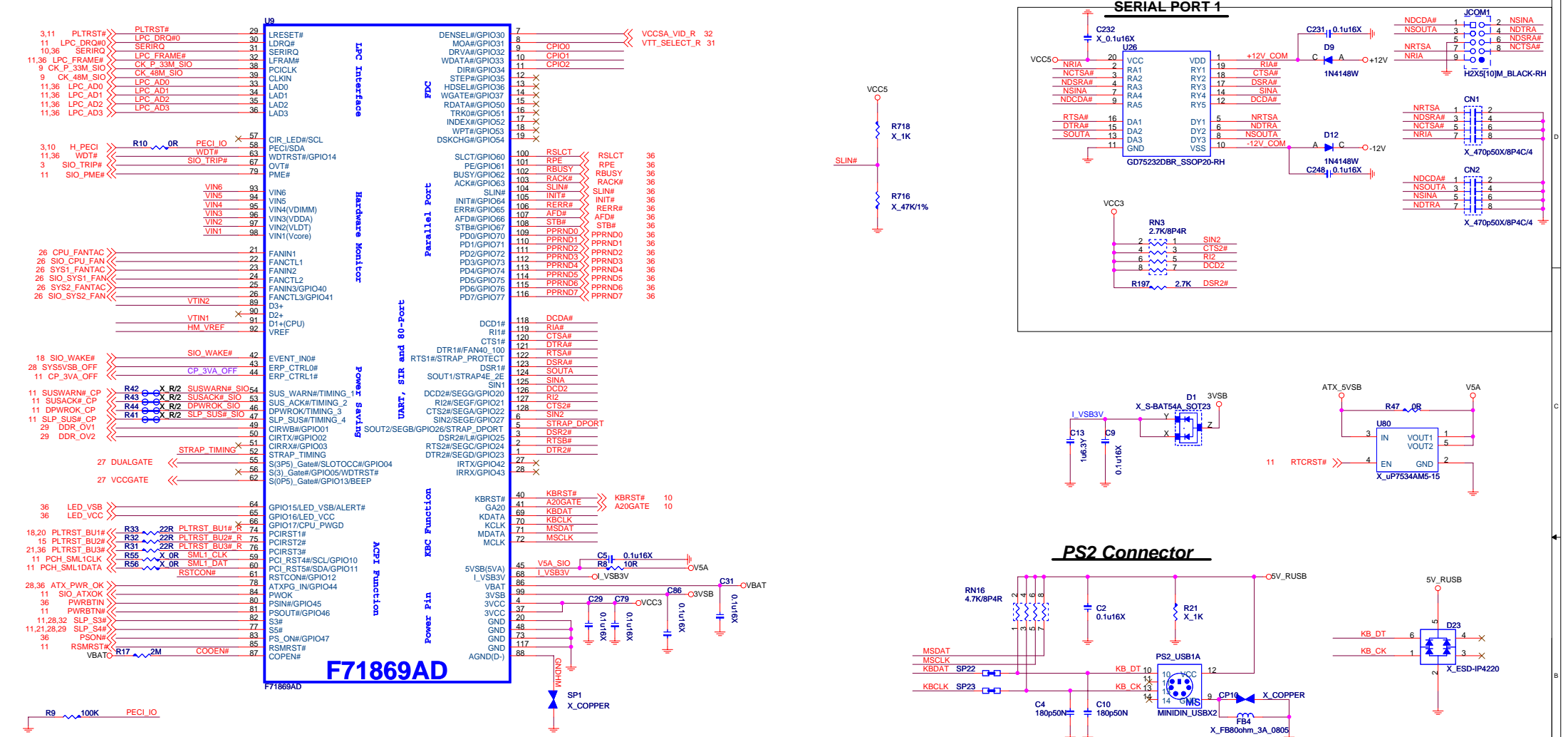
PCI\_Express X16 slot





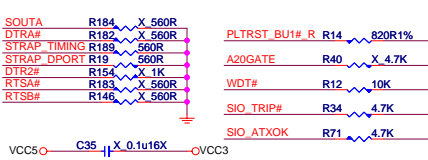
# PCI PULL-UP / DOWN RESISTORS





LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

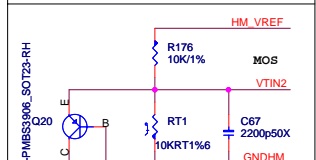
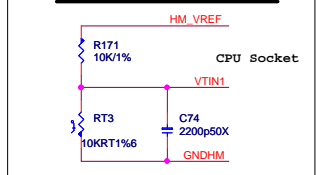
STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 40%	FAN START DUTY 100%
STRAP TIMING	AMD Timing	Intel Courager point Timing
FANCTL 1/2/3	DAC Mode	PWM Mode
STRAP DPORT	Enable 80 Port	Disable 80 Port
RTSA#		



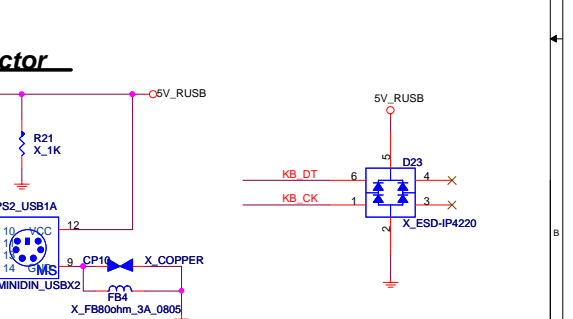
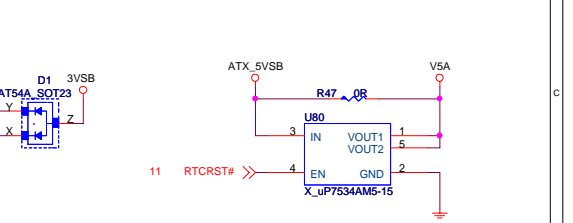
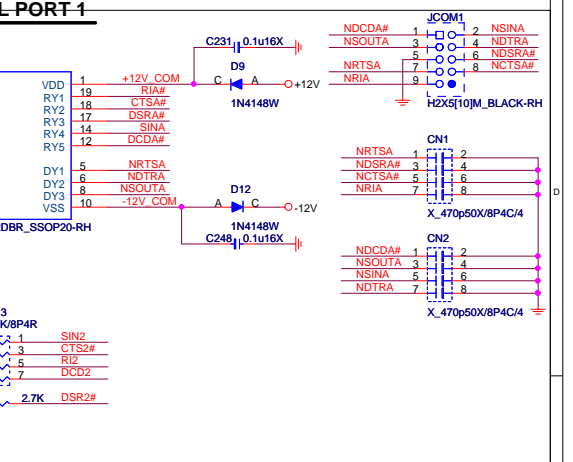
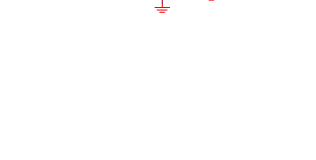
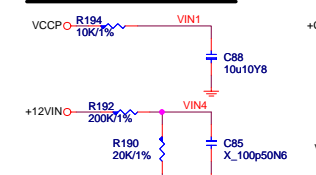
OPT BOM




HW Monitor - Thermal



HW Monitor - Voltage





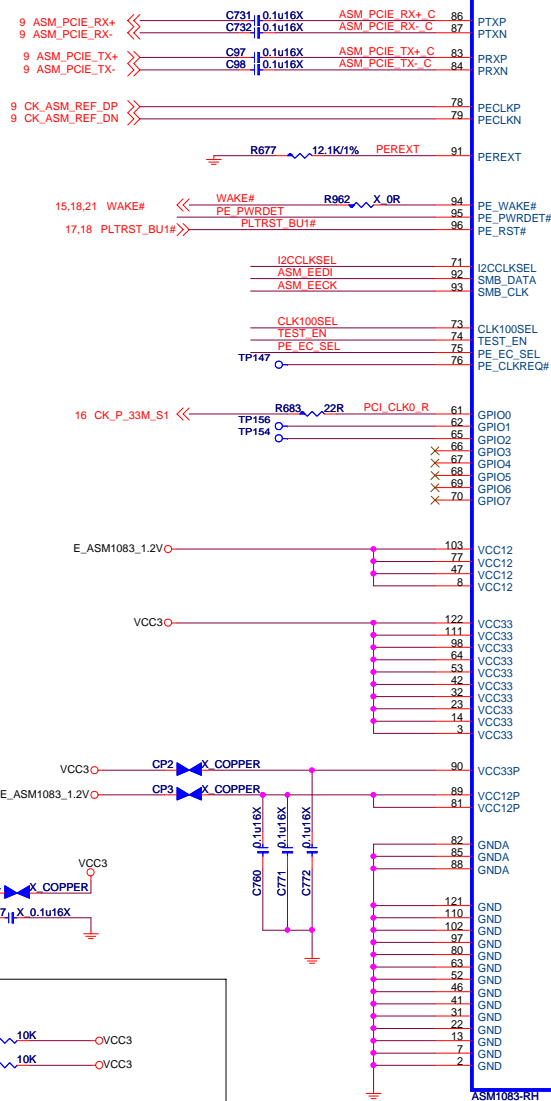
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size	Document Description	Rev
Custom	SIO-Fintek F71869AD(EUP)	2.0
Date: Tuesday, November 16, 2010		Sheet 17 of 39

```
RTL8105E 10/100M LAN
```



<b>MICRO-STAR INT'L CO.,LTD</b>		
<b>MS-7680</b>		
Size Custom	Document Description <b>LAN - RTL8111E / 8105E</b>	Rev 2.0
Date: Tuesday, November 16, 2010		Sheet 18 of 39



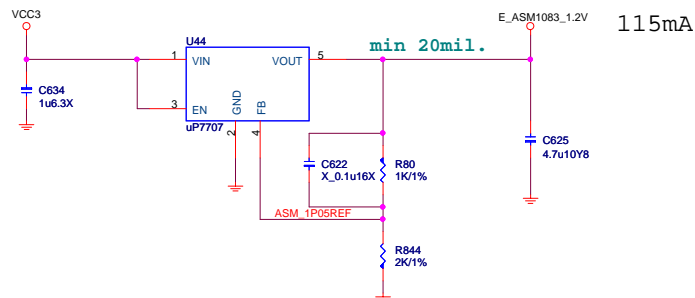


ASM1083

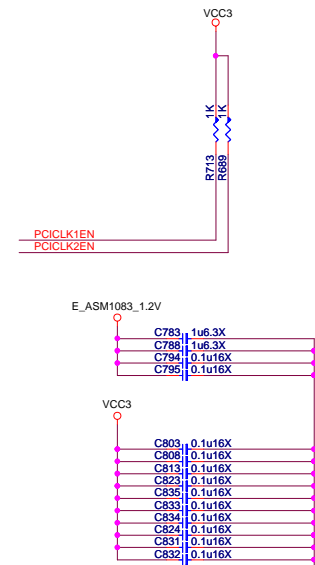
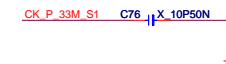
ASM1083-RH

ASM\_EECK R688 10K  
 ASM\_EEDI R727 10K

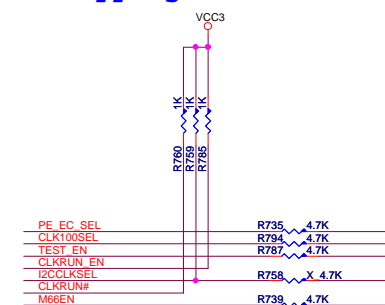
remove EEPROM



EMI



## H/W Strapping



PE\_EC\_SEL-  
 "H" for Express Card mode  
 "L" for PCIe Riser Card mode

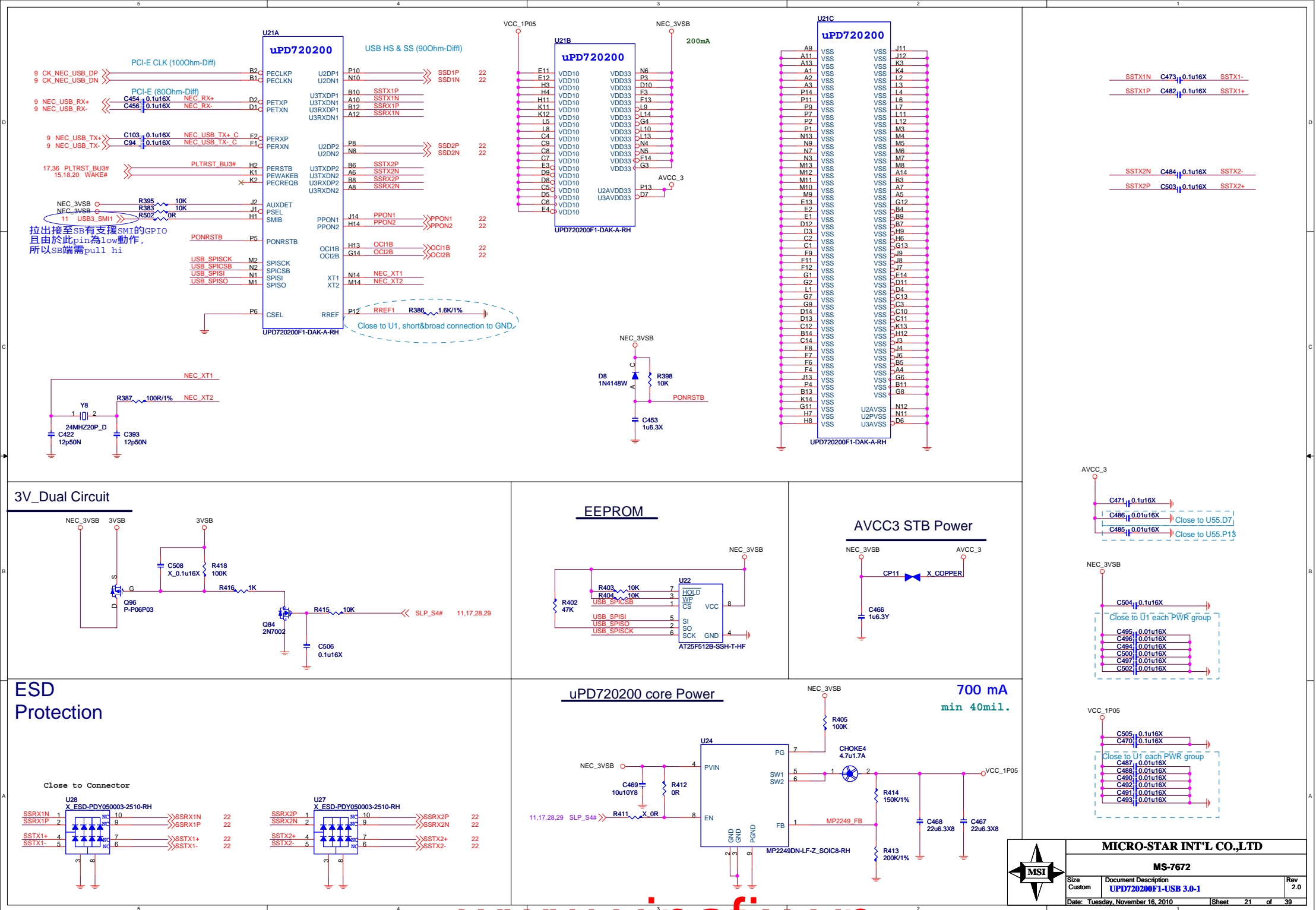
CLK100SEL-  
 "H" for PECLK input only  
 "L" for PECLK & PCICLK input

TEST\_EN-  
 "H" for Test Mode Enable  
 "L" for Test Mode Disable

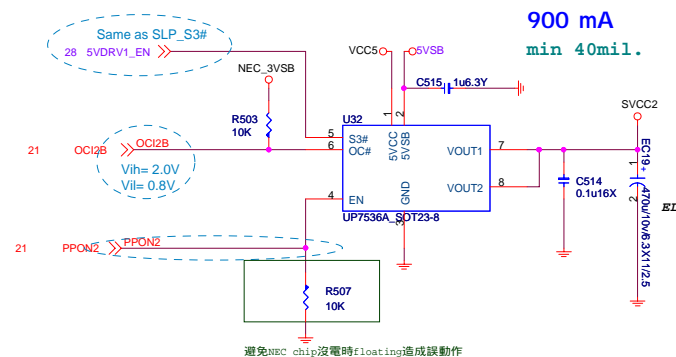
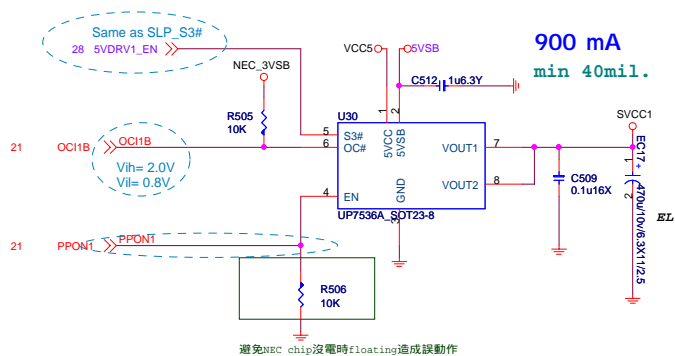
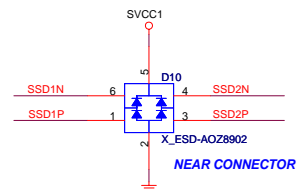
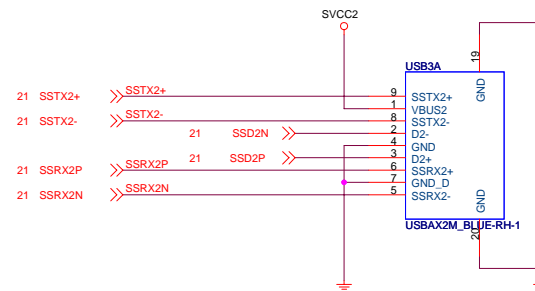
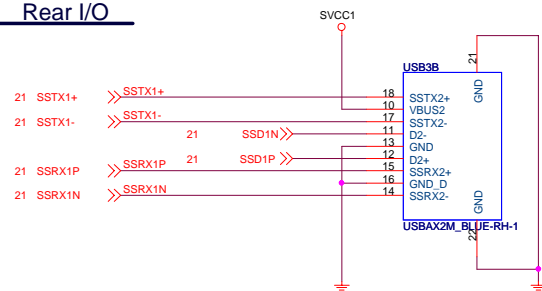
CLKRUN\_EN-  
 "H" for CLKRUN Mode Disable  
 "L" for CLKRUN Mode Enable

I2CCLKSEL-  
 "H" is 135KHz I2CCLK  
 "L" is 67.5KHz I2CCLK

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MS-7672			
Size	Document Description	Rev	
Custom	ASM1083 PCI Brl.	2.0	
Date:	Tuesday, November 16, 2010	Sheet	20 of 39



## Rear I/O

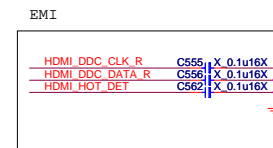
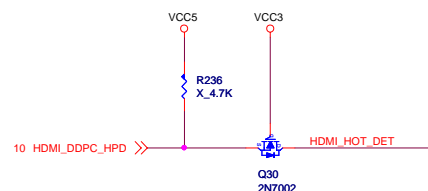
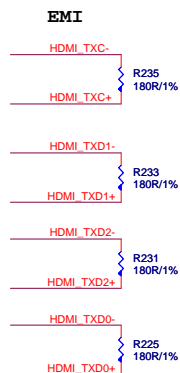
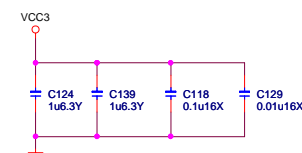
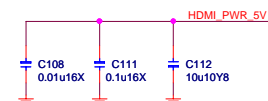
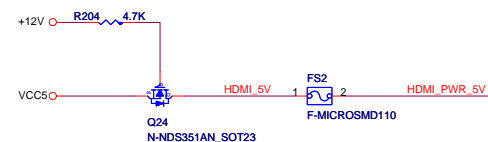
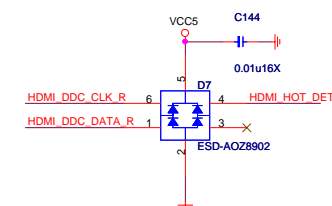
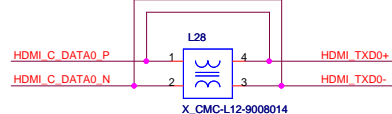


All power sources of uPD720200 are supplied, PPONx is enable.  
PPONx is low when OC1x going to low.

MICRO-STAR INT'L CO.,LTD			
MS-7672			
Size	Document Description	Rev	
Custom	USB 3.0 Power & Connector	2.0	
Date:	Tuesday, November 16, 2010	Sheet	22 of 39



HDMI, DVI : 1920x1200 at 60 Hz (16:10 WUXGA)



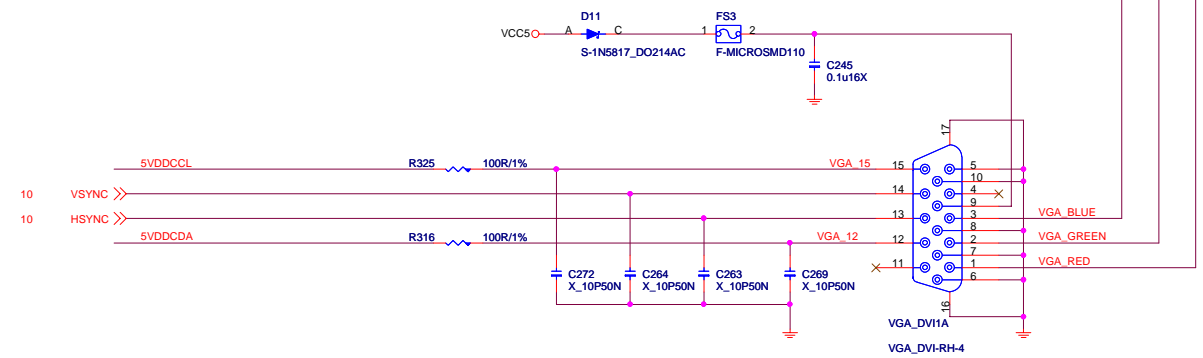
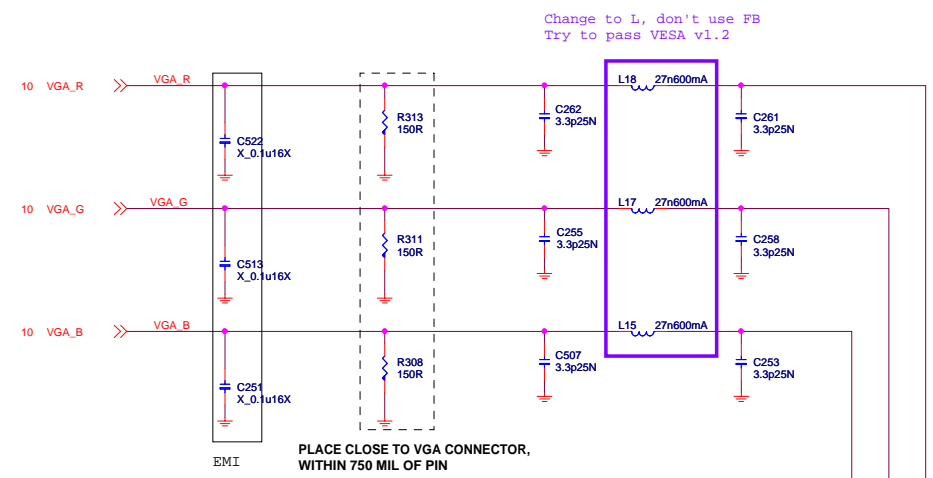
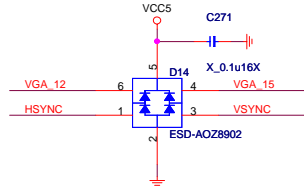
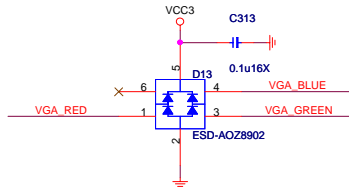
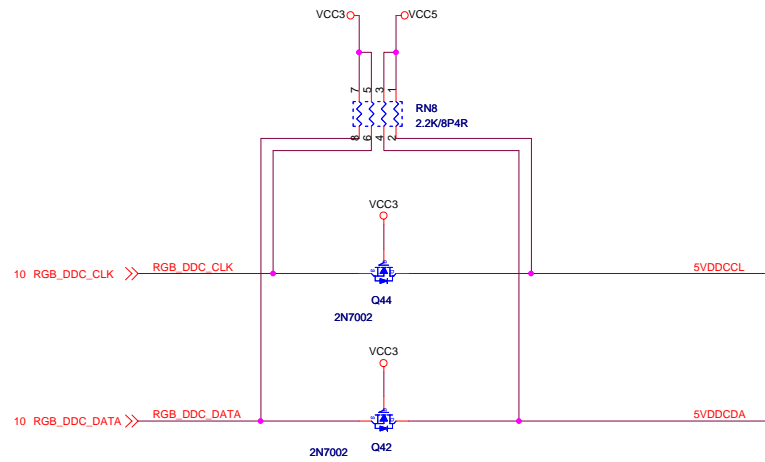
MS-7680

Size Custom	Document Description <b>HDMI</b>	Rev 2.0
Date: Tuesday, November 16, 2010		Sheet 24 of 39

D-Sub

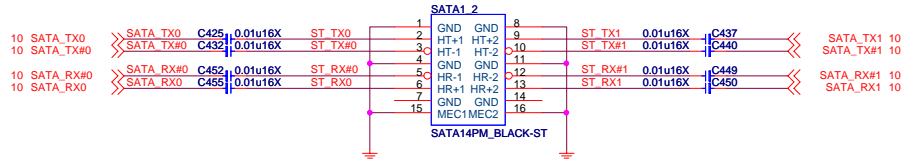
VGA: resolution of 2048x1536 pixels with 32-bit color at 75 Hz (4:3 QXGA)

Level shift

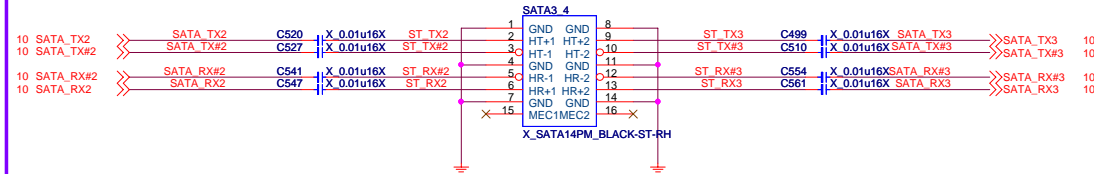


## SATA 6G PORT 0,1

H61 PORT 0/1 Support 3G  
H67 PORT 0/1 Support 6G



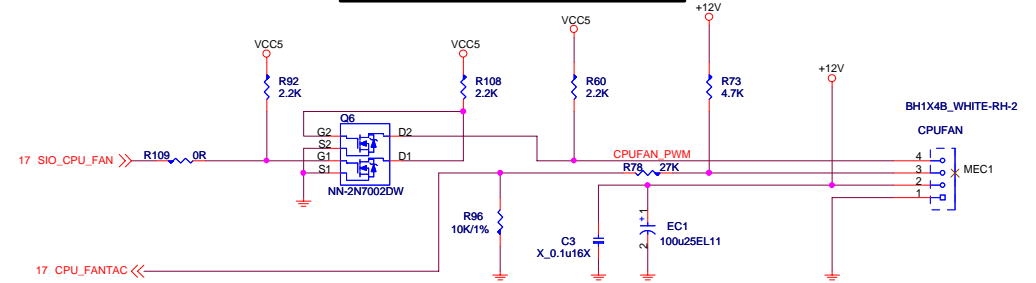
## SATA 3G PORT 2,3



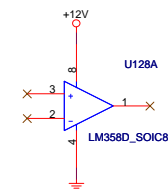
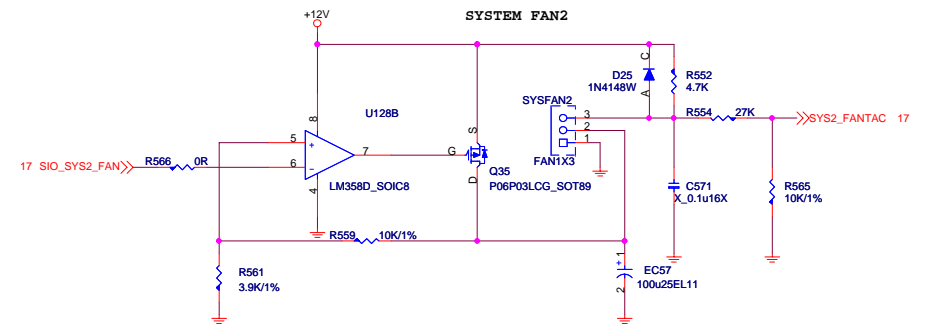
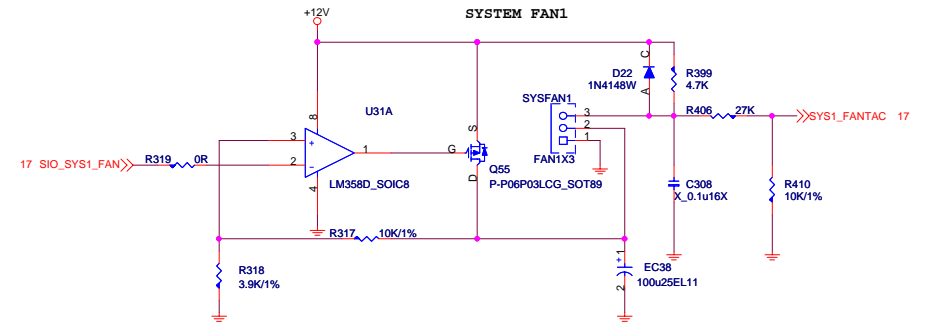
For H61,SATA3&4 removed



## CPU FAN-COUNTROL CIRCUIT



## SYSTEM FAN-COUNTROL CIRCUIT



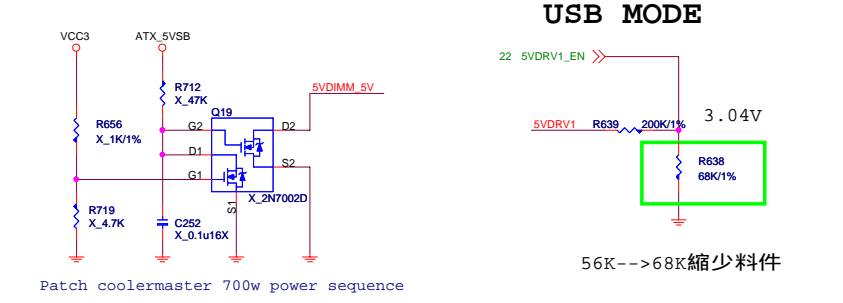
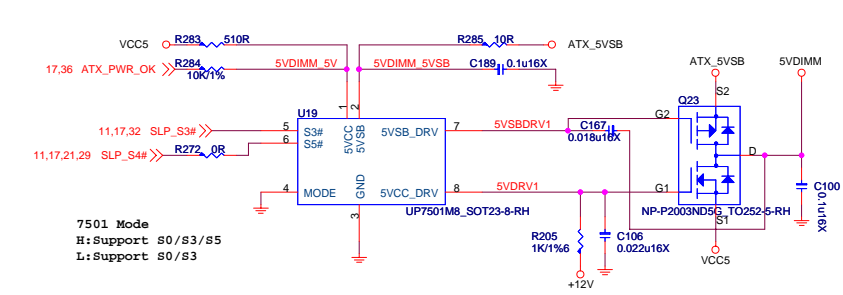
MICRO-STAR INT'L CO.,LTD

MS-7680

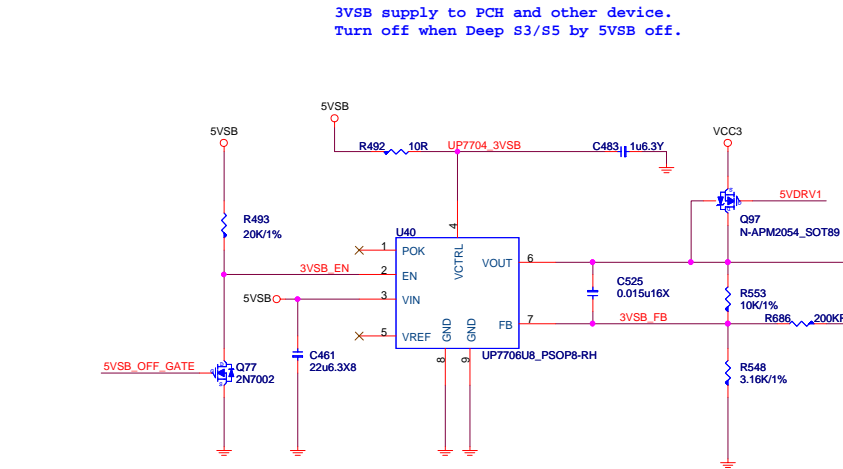
Size	Document Description	Rev
Custom	SATA / FAN Control	2.0
Date: Tuesday, November 16, 2010	Sheet 26 of 39	



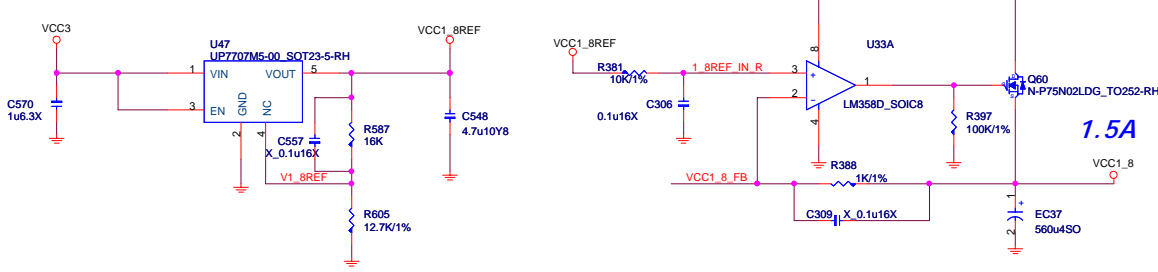
5VDIMM FOR DDR



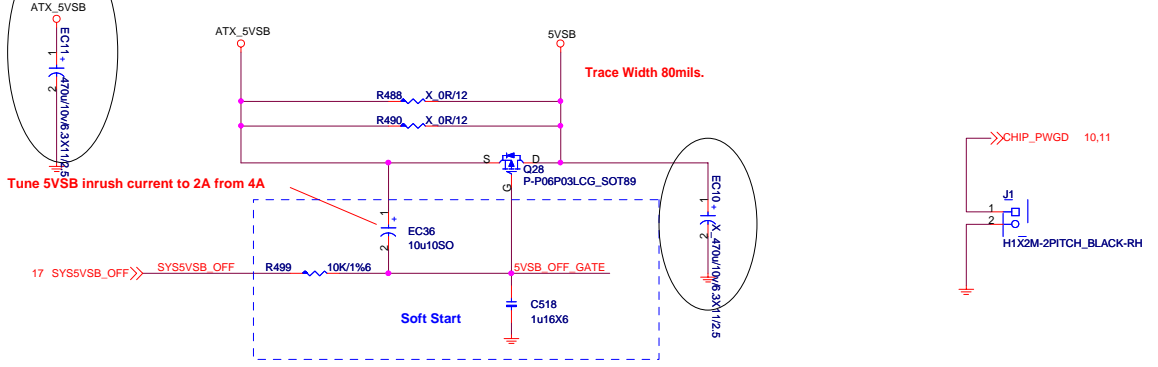
3VSB



VCC1\_8REF



5VSB Power Switch



**JPI:**

**EUP Disable:**

1,2 Support Wake up Function

2,3 not Support Wake up Function

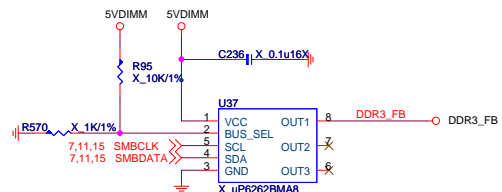
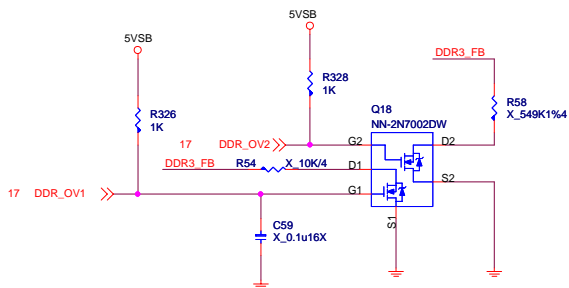
**EUP Enable:**

not Support Wake up Function

DDR3\_1.5V 4.5A+7.5A+1A=13A

4.5A FOR CPU  
7.5A FOR 2DIMM  
1A FOR DDR VTT

OV

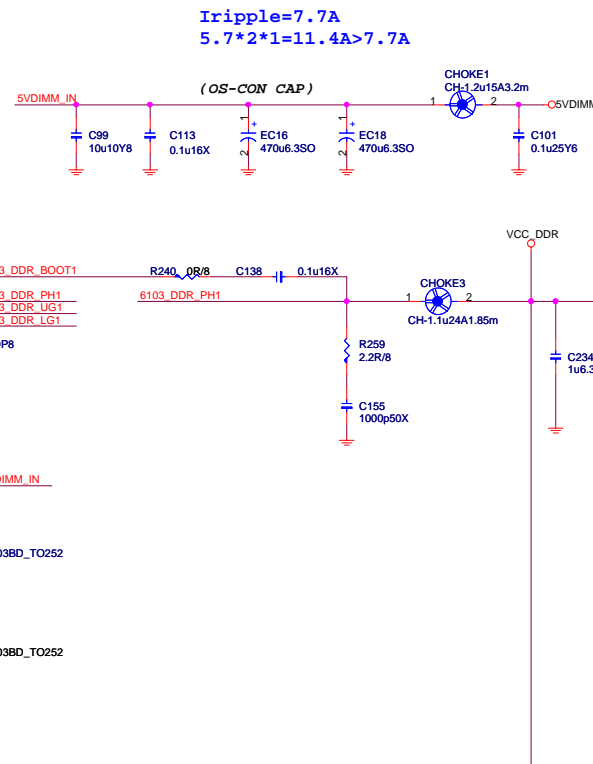
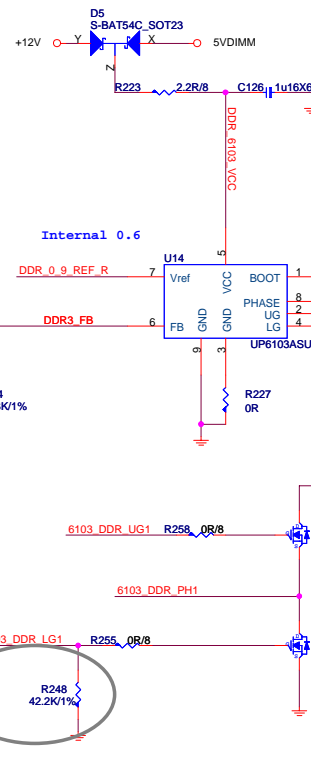
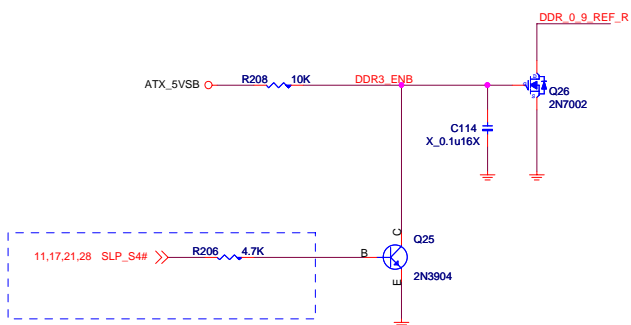


### UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

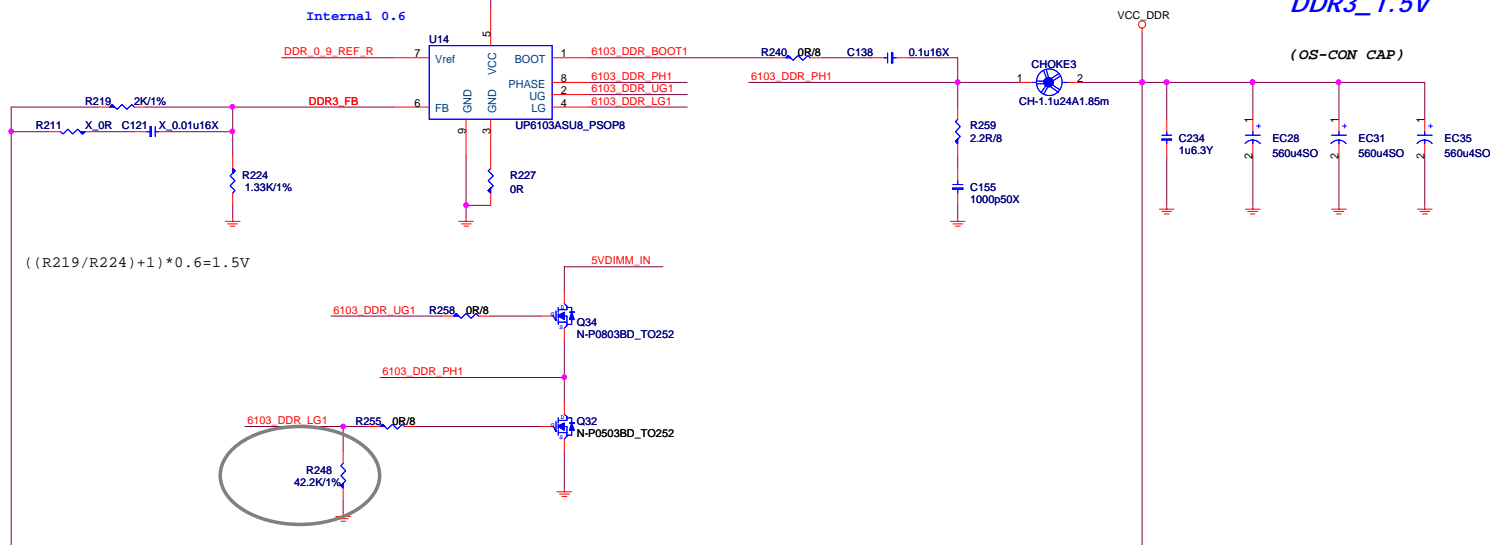
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

P.S. Only for meet Intel power down sequence.



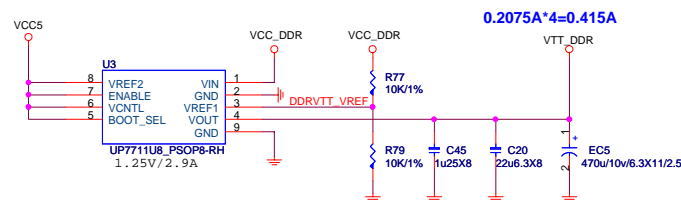
Tripple=7.7A  
5.7\*2\*1=11.4A>7.7A

DDR3\_1.5V



### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

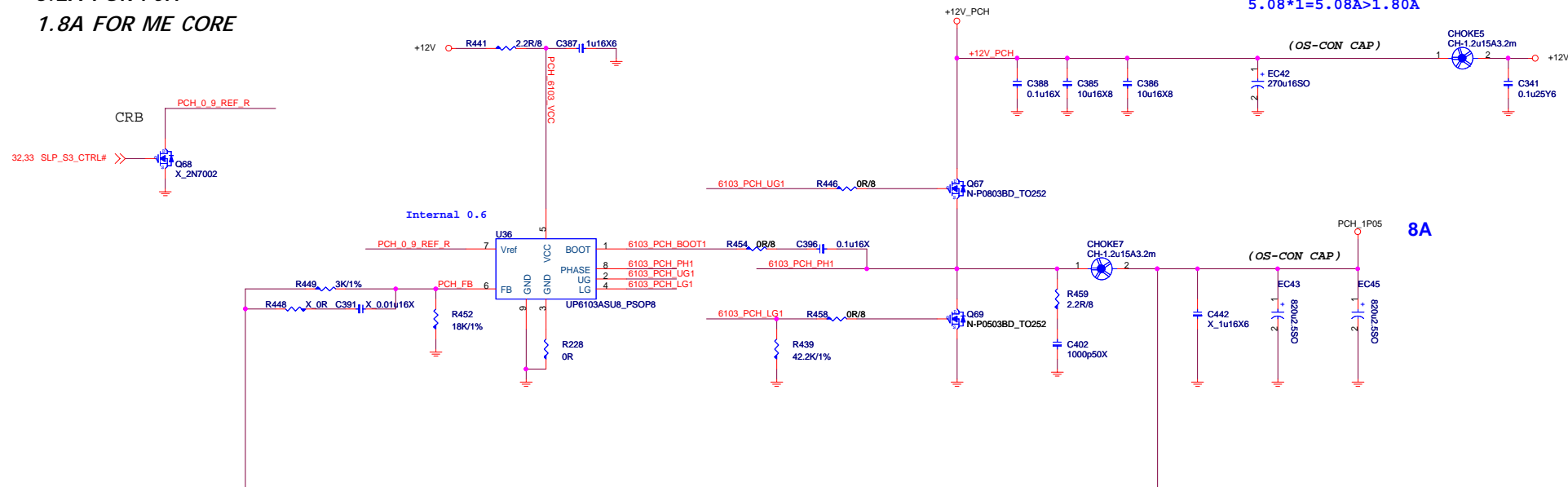


MICRO-STAR INT'L CO.,LTD

MS-7680

Size	Document Description	Rev
Custom	DDR Power - uP6103 1-Phase	2.0
Date:	Tuesday, November 16, 2010	Sheet 29 of 39

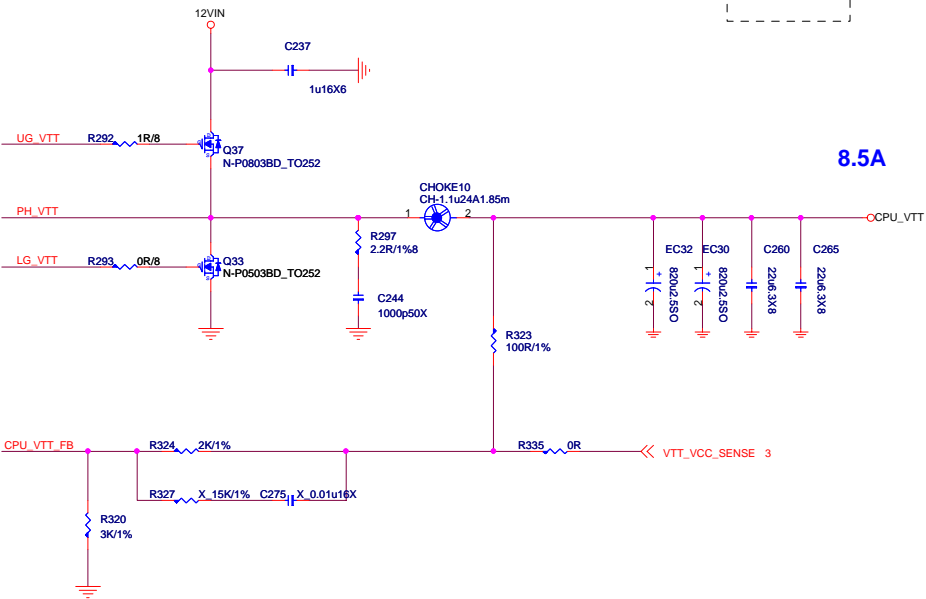
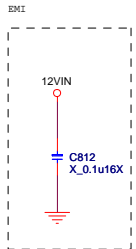
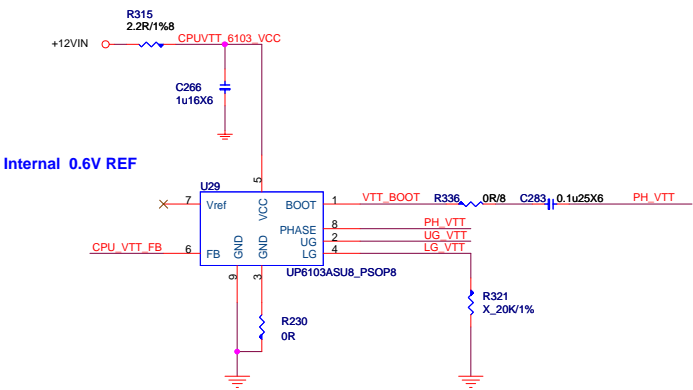
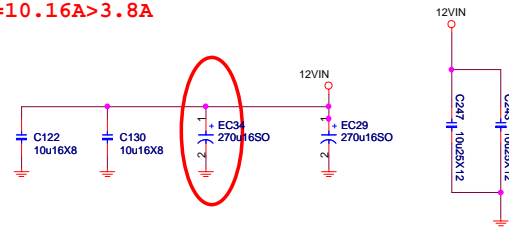
**1.8A FOR ME CORE**



# CPU\_VTT:1.05/1.00

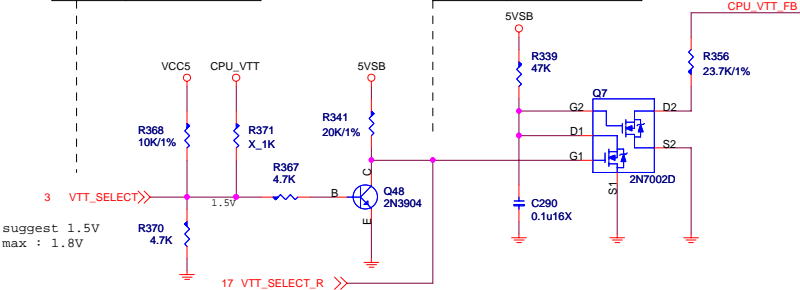
$CPU\ VTT\ 8.5A + SA\ Core = 8.8A = 17.3A$

$I_{ripple} = 1.92(vtt) + 1.88(sa)$   
 $5.08 * 2 = 10.16A > 3.8A$



VTT_SELECT	
Low	1.0V
High	1.05V

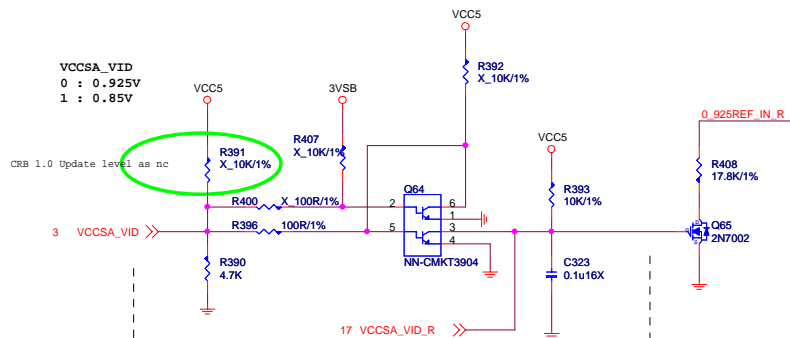
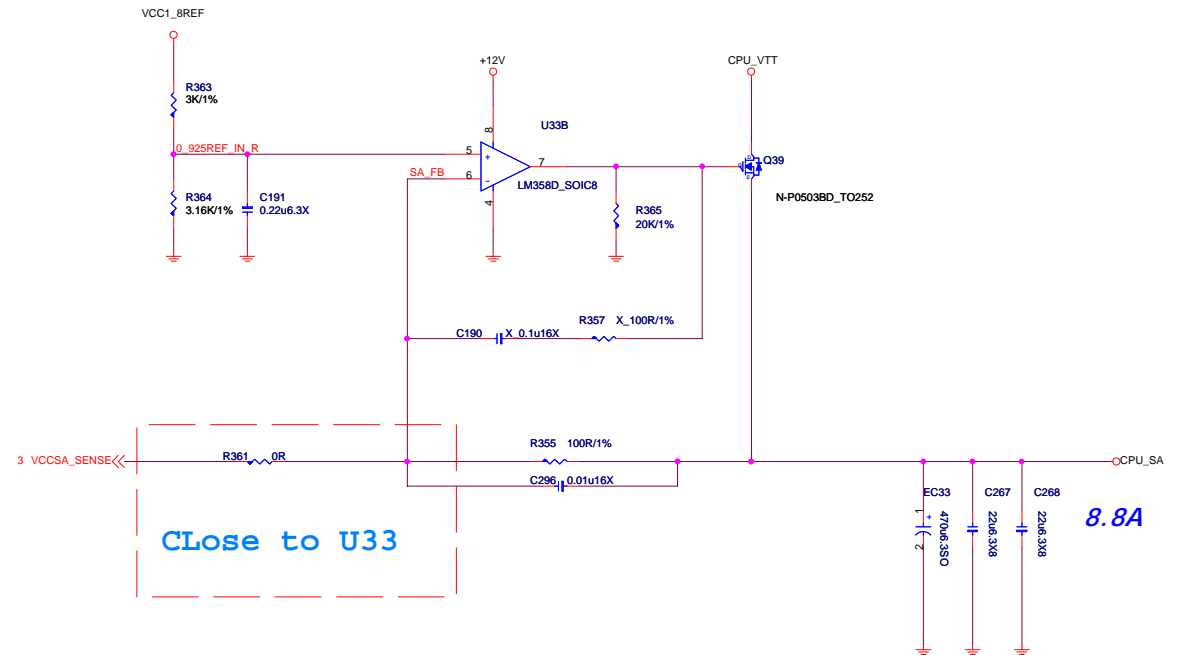
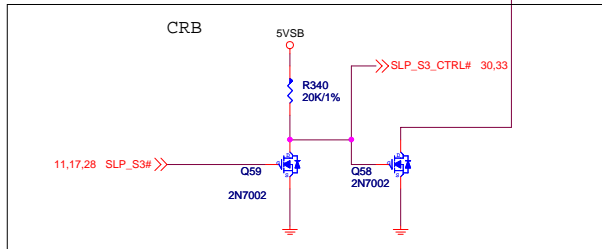
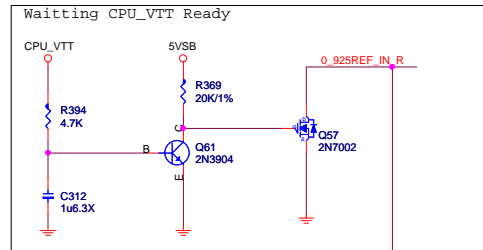
VTT_SELECT Table	
Low	1.05V
High	1.0V



MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size	Document Description	Rev
Custom	CPU_VTT - uP6103- 1-Phase	2.0
Date:	Tuesday, November 16, 2010	Sheet 31 of 39

# CPU\_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V

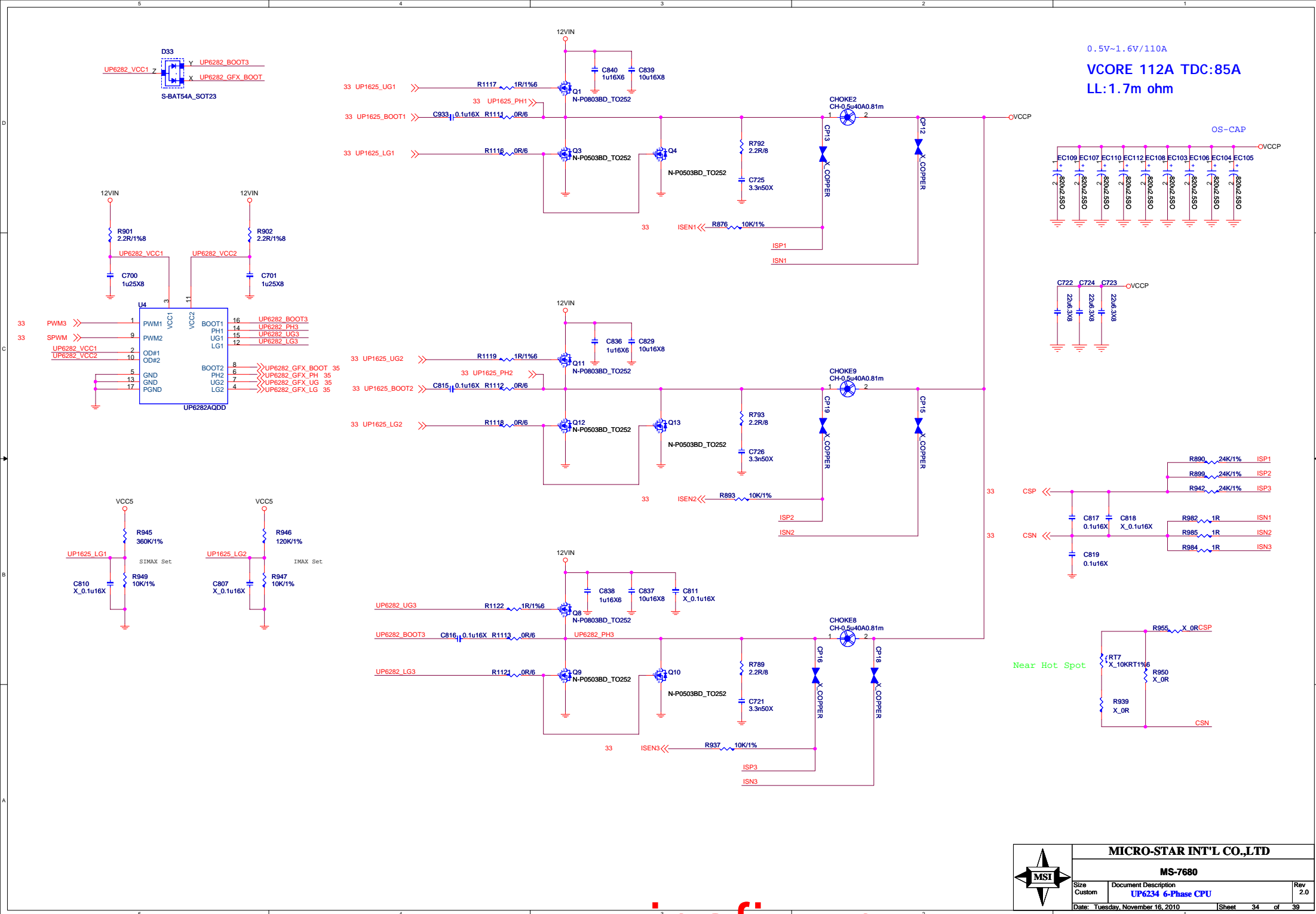


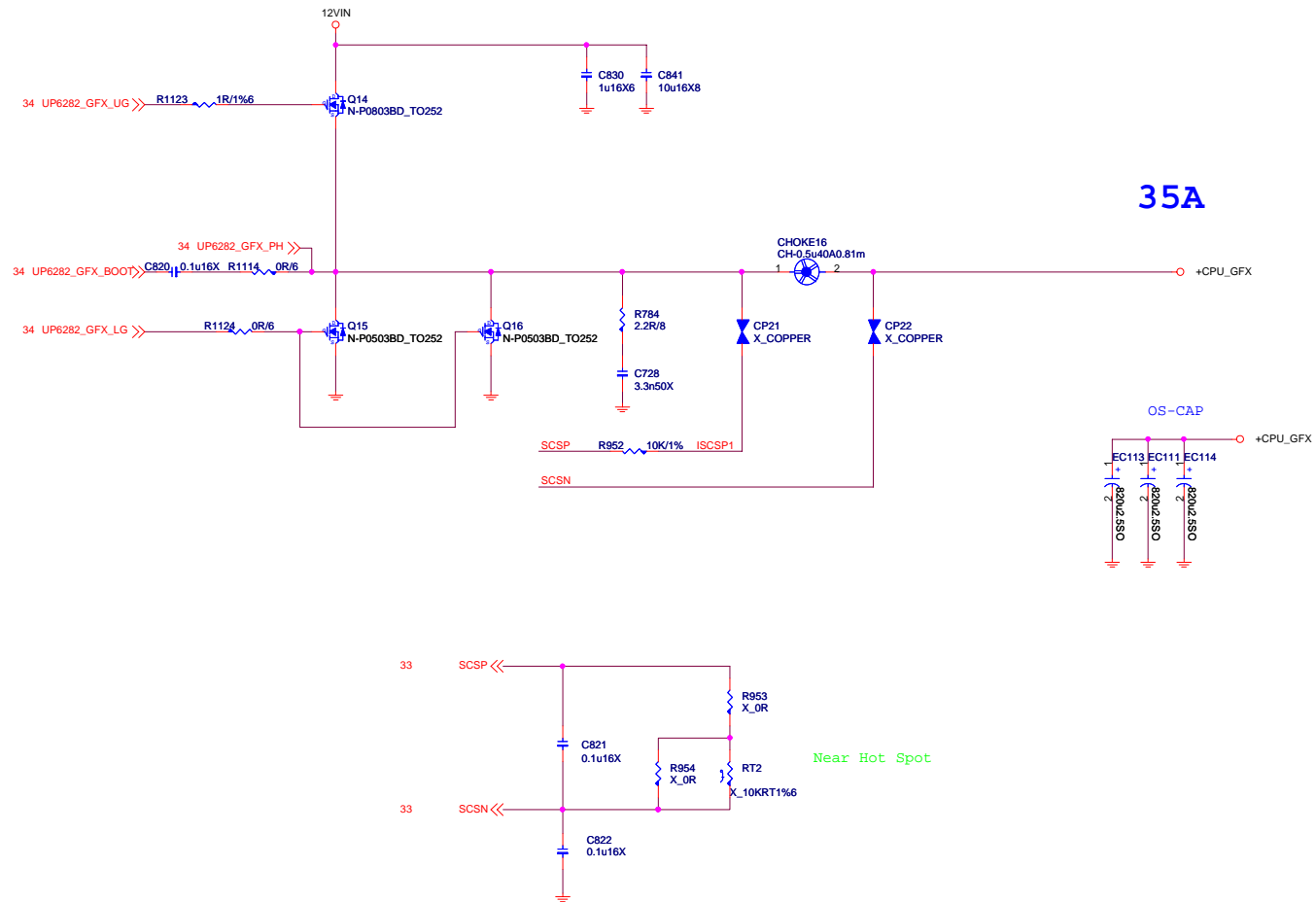
MICRO-STAR INT'L CO.,LTD

MS-7680

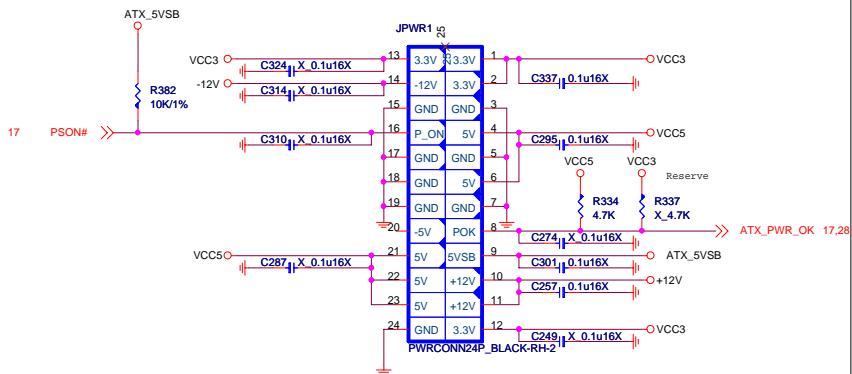
Size	Document Description	Rev
Custom	CPU_SA - uP6103 1-Phase	2.0
Date:	Tuesday, November 16, 2010	Sheet 32 of 39



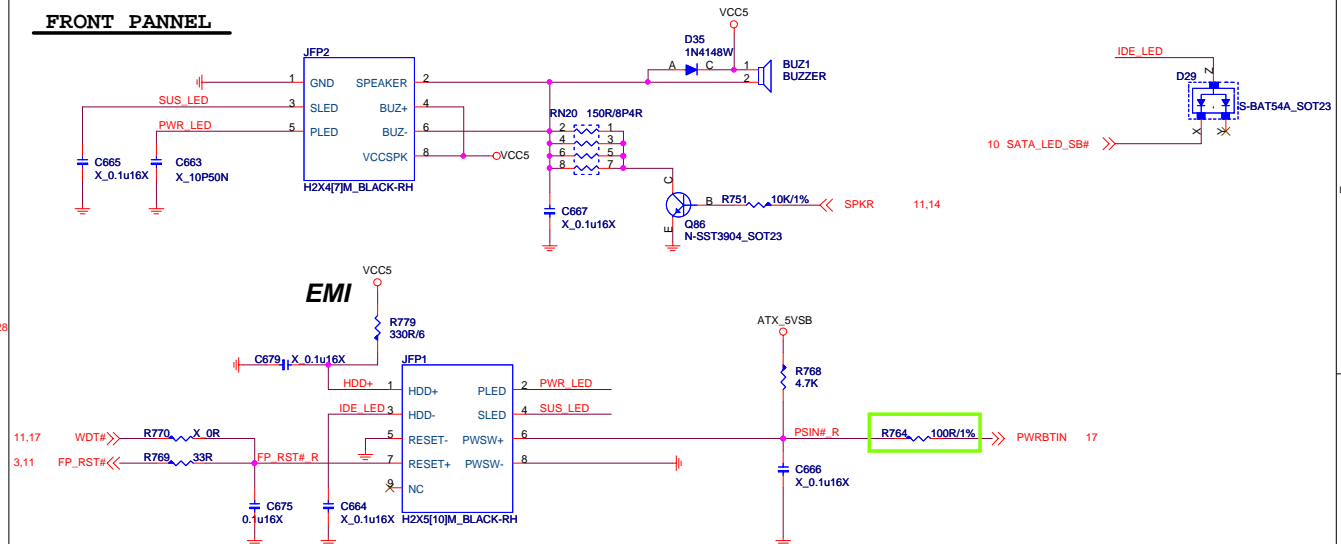




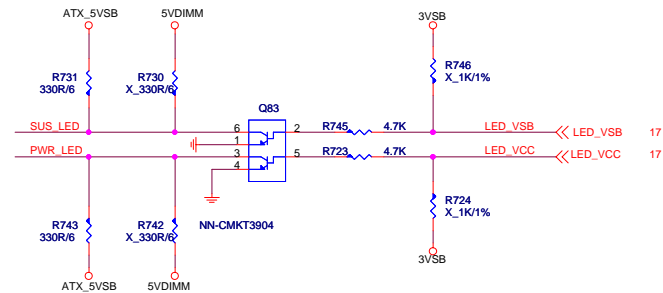
## ATX POWER CONNECTOR



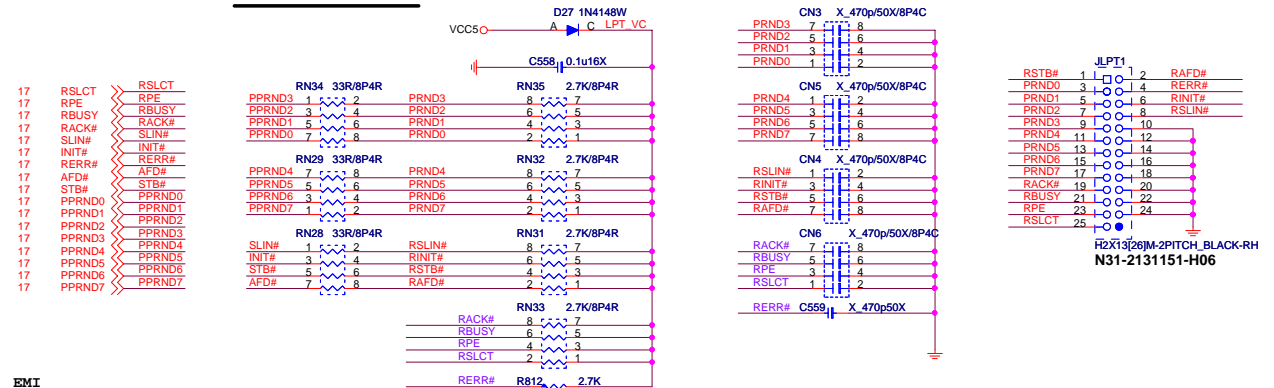
FRONT PANNEL



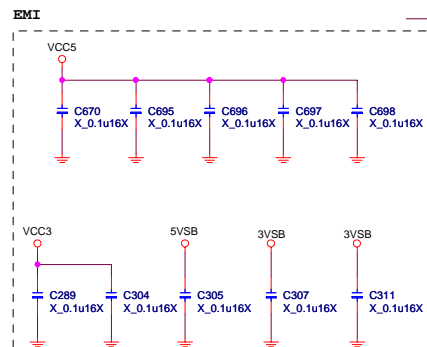
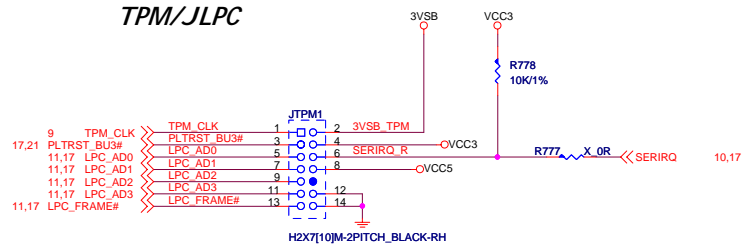
LED ( for Fintek 71889)



## PARALLAL PORT

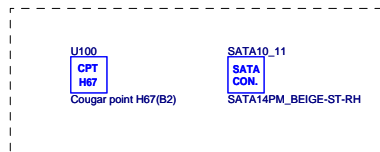


## TPM/JLPC

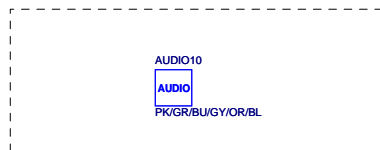


<b>MICRO-STAR INT'L CO.,LTD</b>			
<b>MS-7680</b>			
Size Custom	Document Description <b><u>ATX PWR-Connector &amp; Front Panel &amp; EMI</u></b>		Rev 2.0
Date: Tuesday, November 16, 2010		Sheet 36 of 39	

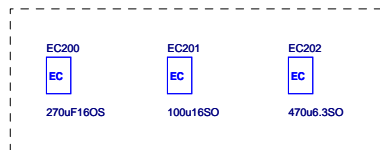
### H67 OPT.



### AUDIO CON OPT.



### EL/OS OPT.



7680-20

PK0-0768020-G37, 精成, 23, 寶安思斯通廠 (MSIS), 4, Coffee  
 PK0-0768020-G37, 精成, 32, 寶安思斯通廠 (MSIS), 4, Coffee  
 PK0-0768020-E36, E&E, 23, 寶安思斯通廠 (MSIS), 4, Coffee  
 PK0-0768020-E36, E&E, 22, 寶安思斯通廠 (MSIS), 4, Coffee



BAT-BCR2032P-RH



RUB1



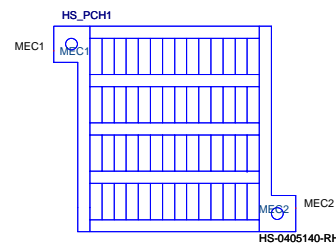
RUB2



CPU 鐵座

E21-7557040-L06

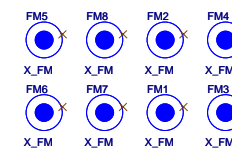
### PCH XDP PWRGD/RESET



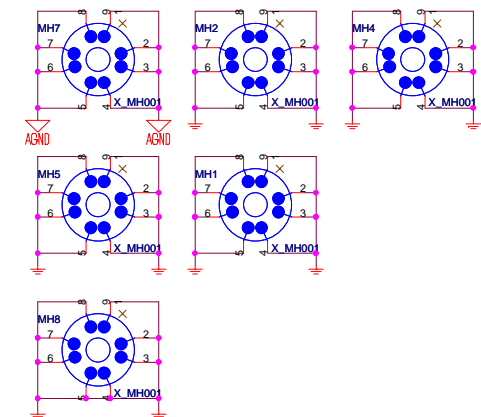
### Simulation



### Optical Fiducial Marks-120



### Mounting Holes



MICRO-STAR INT'L CO.,LTD			
MS-7680			
Size Custom	Document Description XDP / Manual Parts		Rev 2.0
Date: Tuesday, November 16, 2010	Sheet	37	of 39